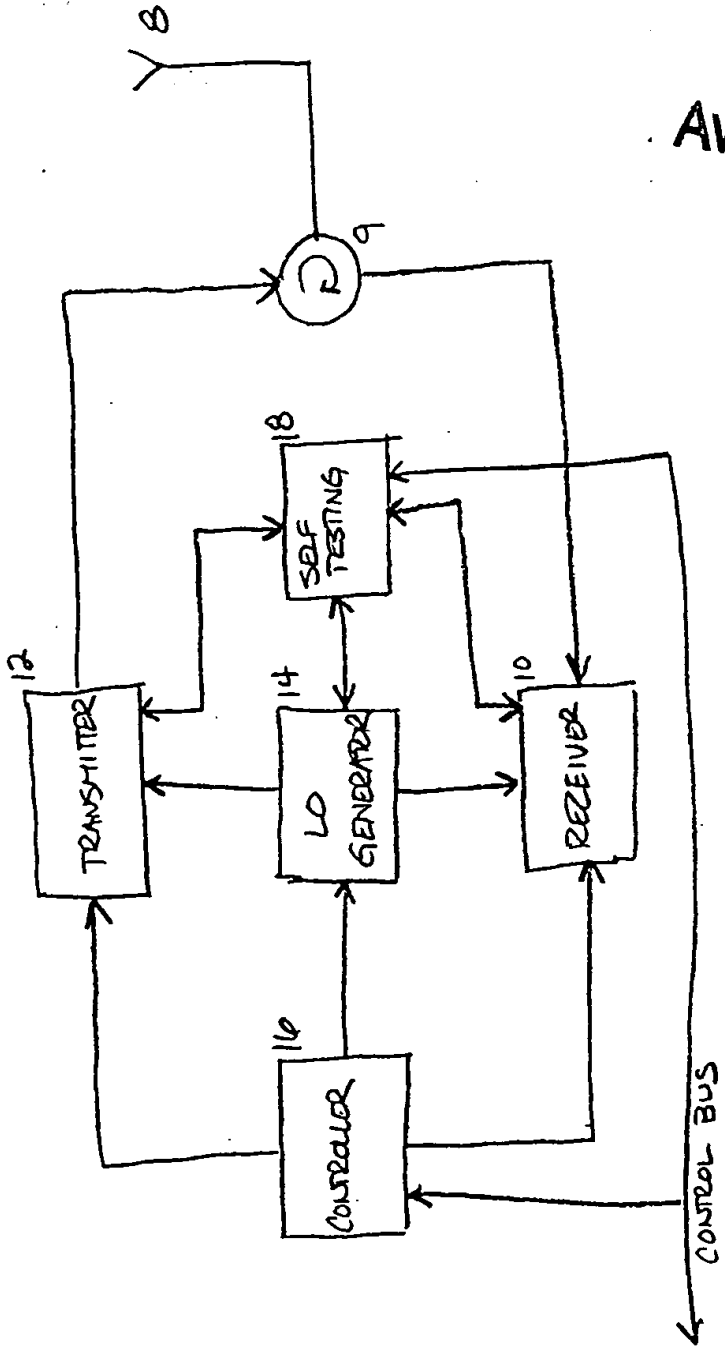


Available Copy

FIG. 1A



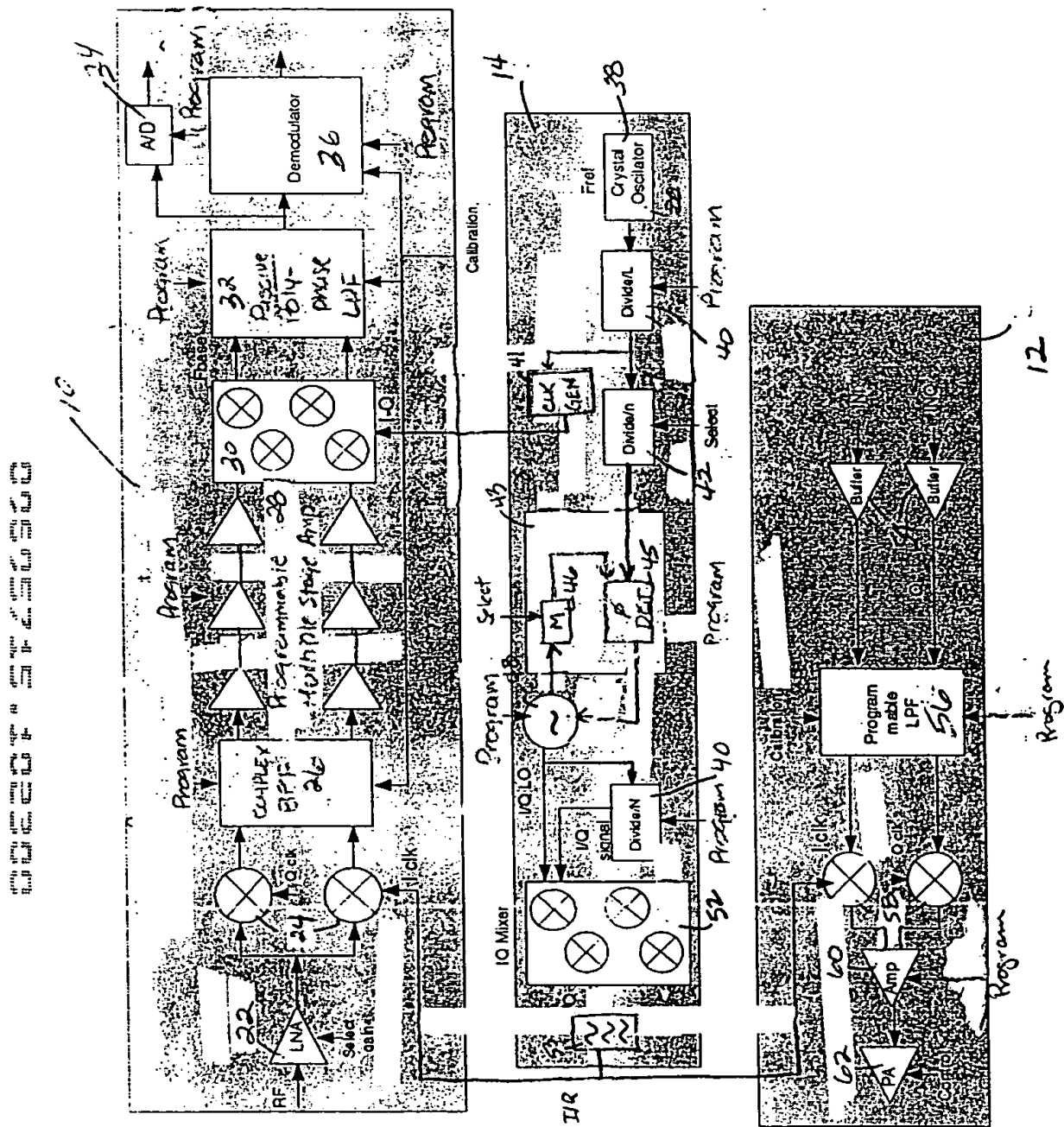


Fig. 2

FIG. 3 is a block diagram of a system 52.

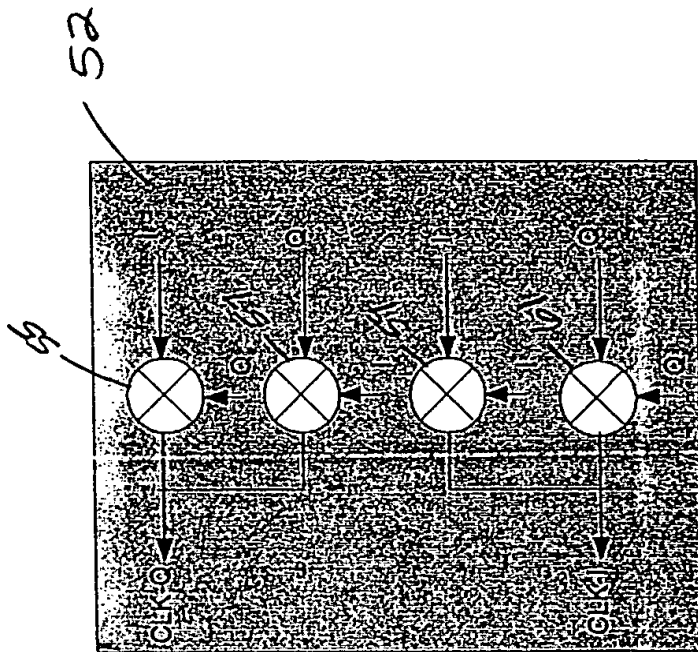


FIG. 3

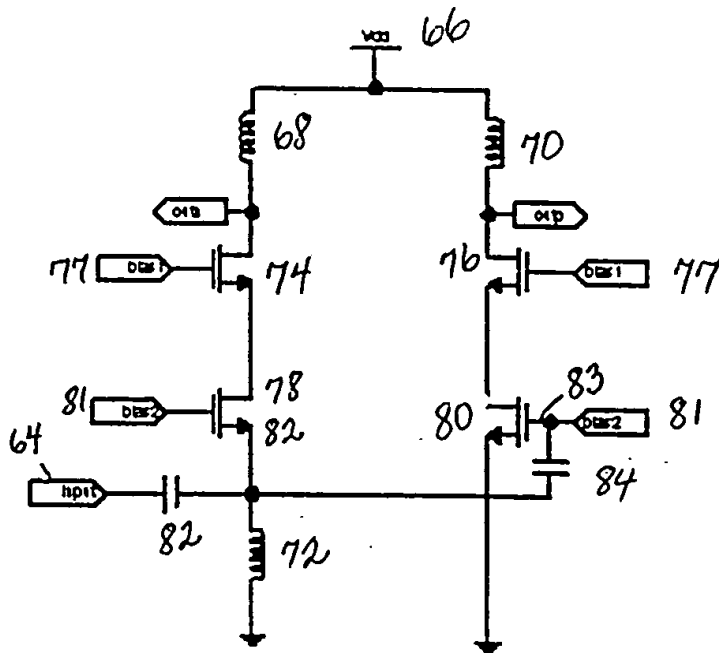


FIG. 4

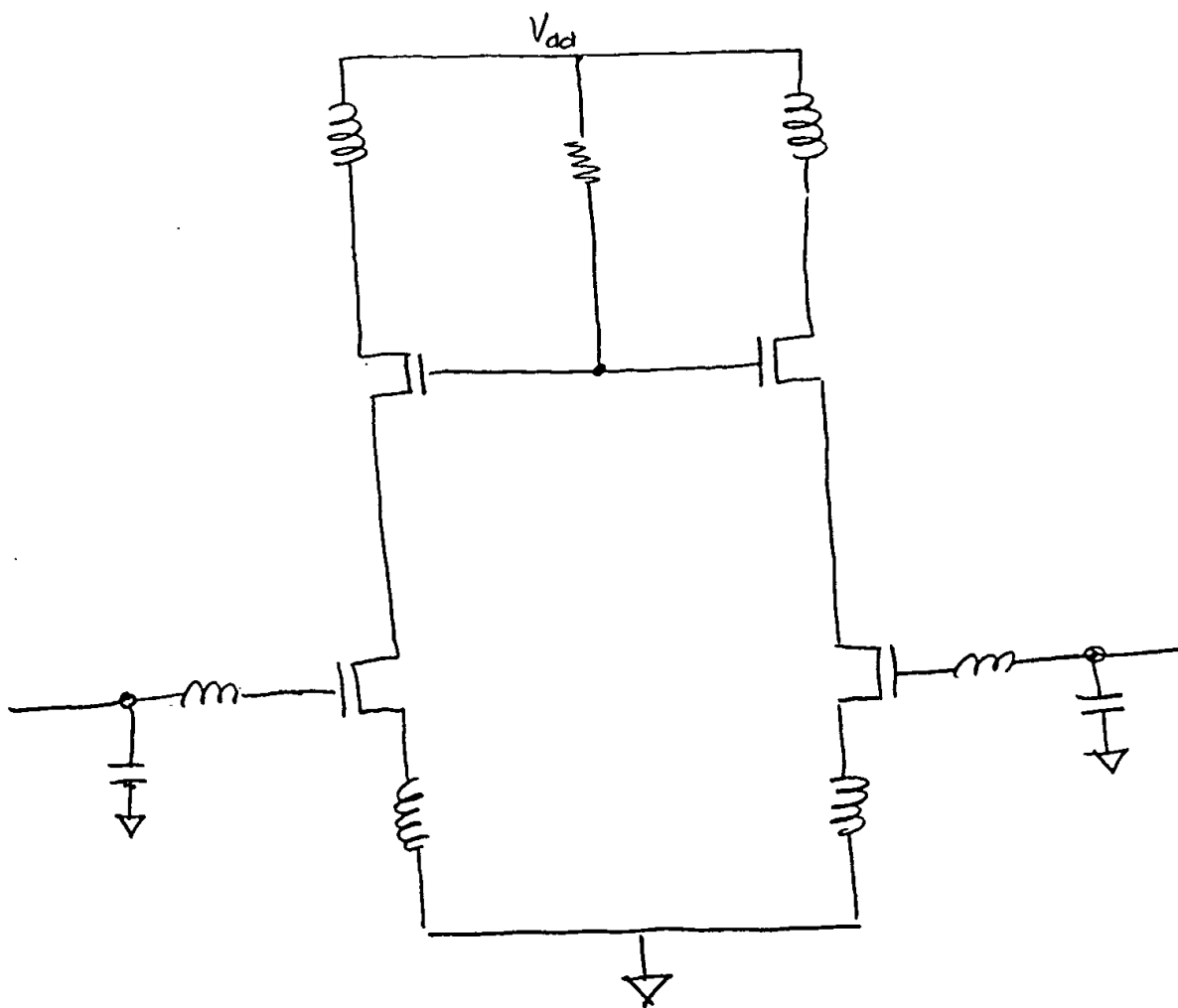


FIG. 4(a)

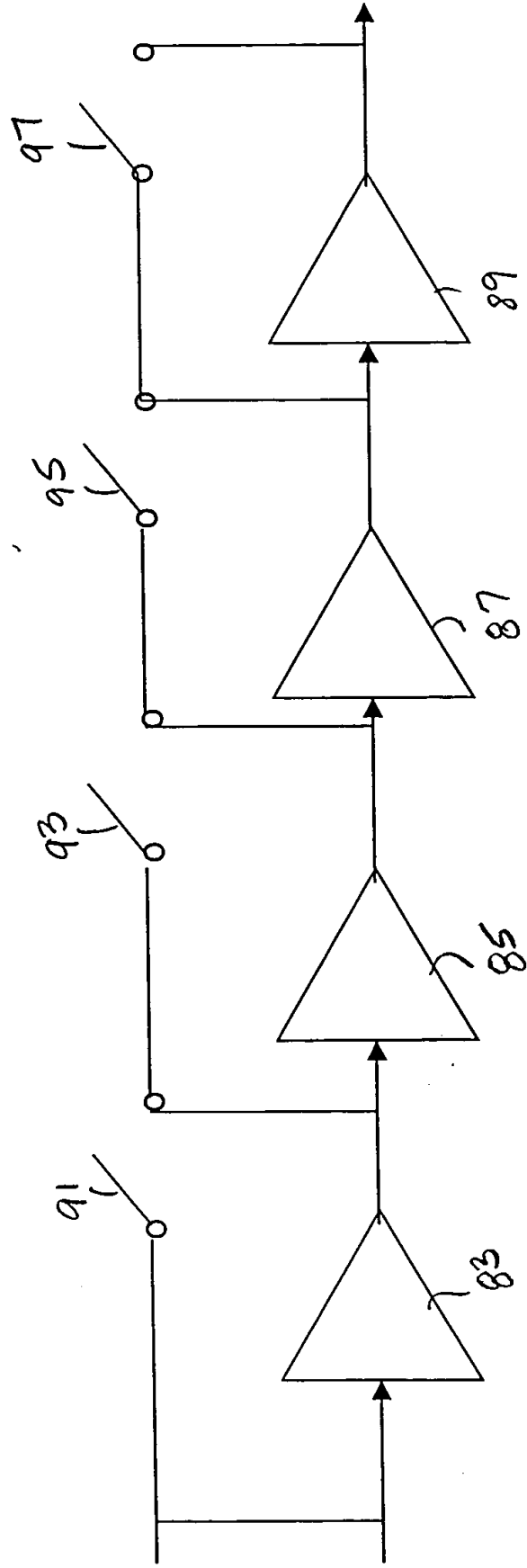


FIG. 5



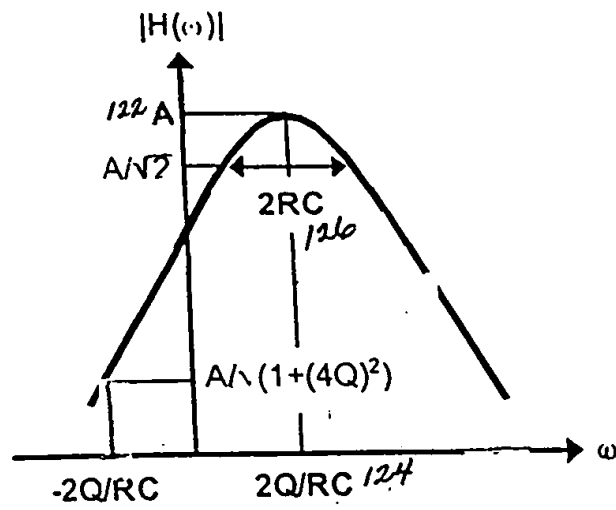


FIG. 7



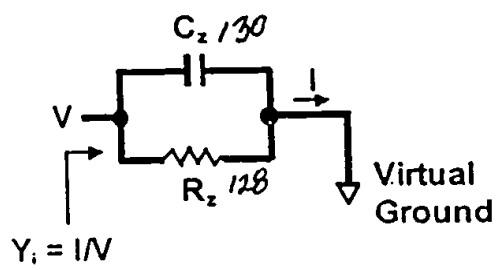


FIG. 8

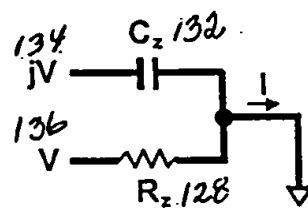


FIG. 9

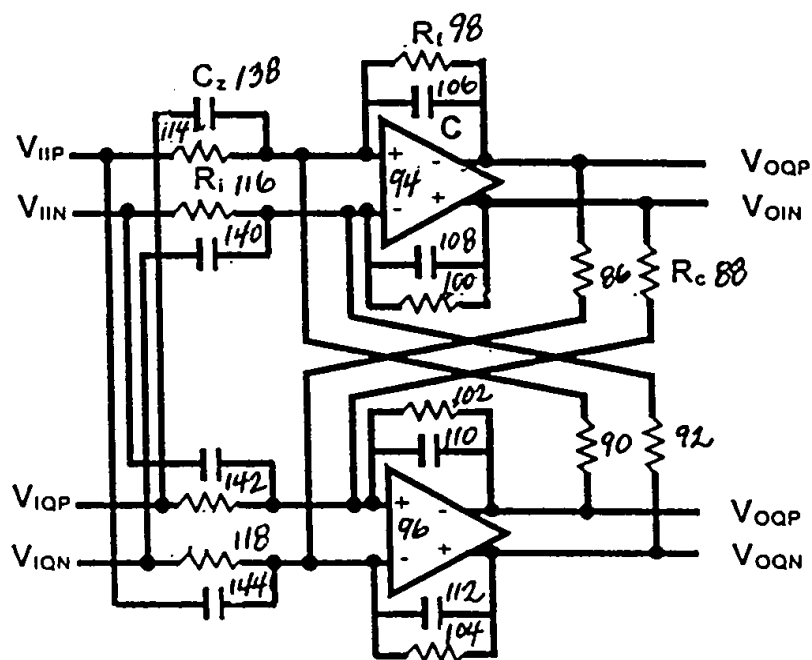


FIG. 10

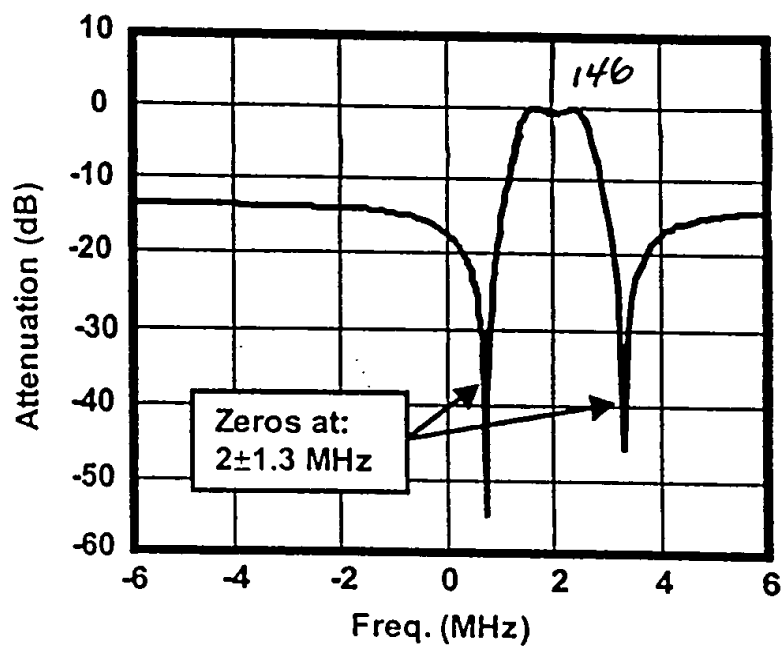


FIG. 11

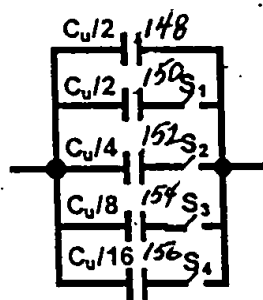


FIG. 12(a)

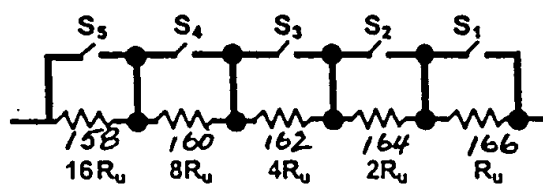


FIG. 12(b)

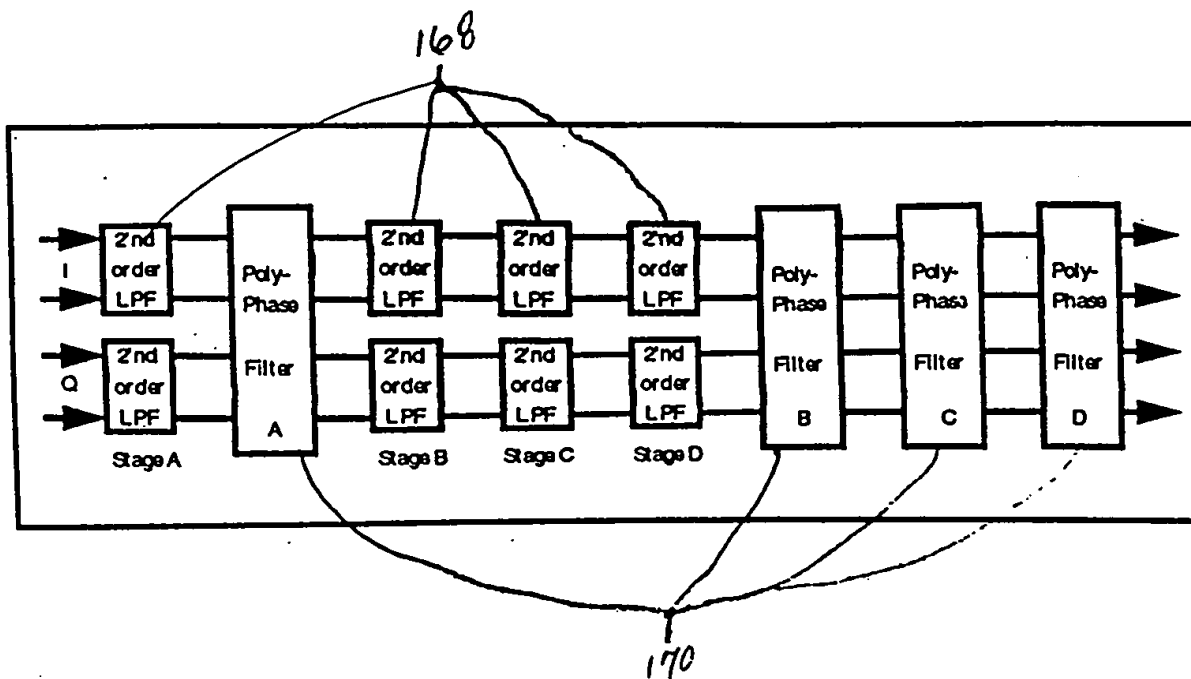


FIG. 13

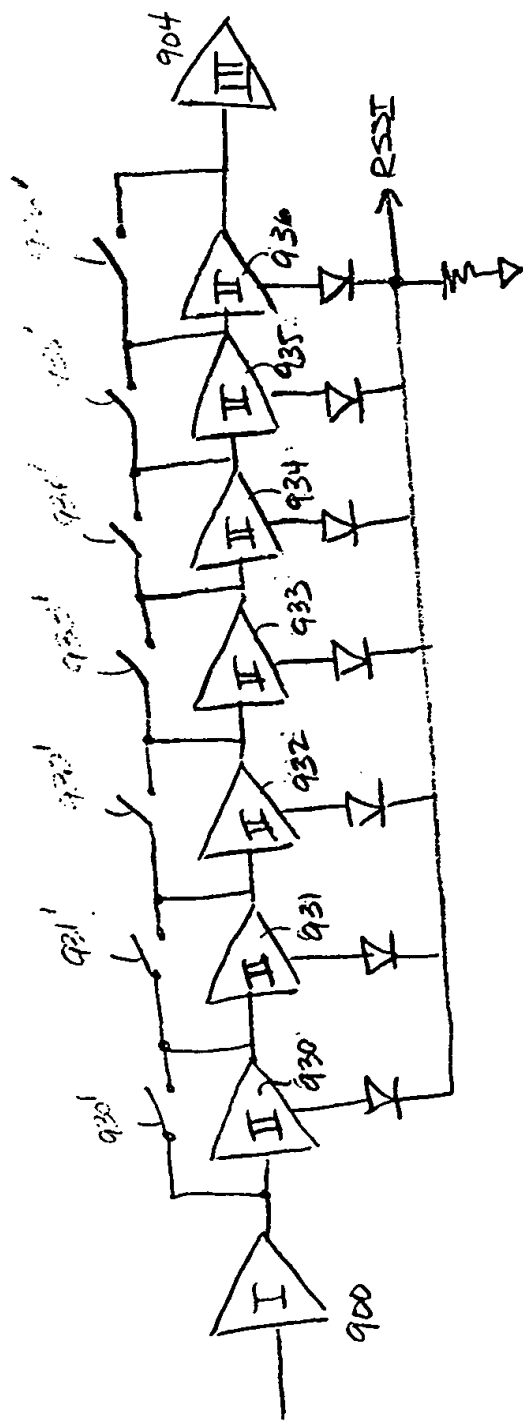
[illegible]

FIG. 14

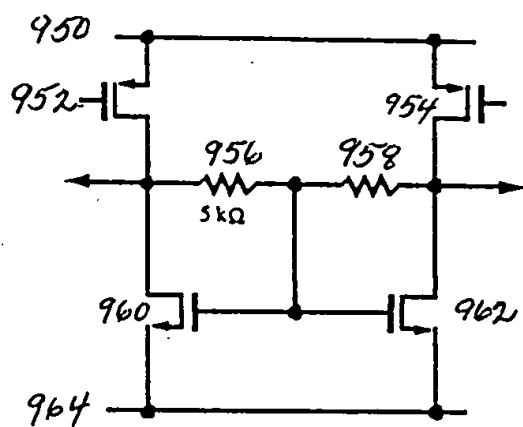


FIG. 15

The diagram shows a 4-bit ripple-carry adder circuit. It is composed of four full-adder blocks connected in series. The top input is labeled 864, the bottom input is 950, and the carry-in is 952. The outputs are labeled 860, 862, 957, 958, and 955.

FIG. 16(a)



↗

FIG. 17(a)

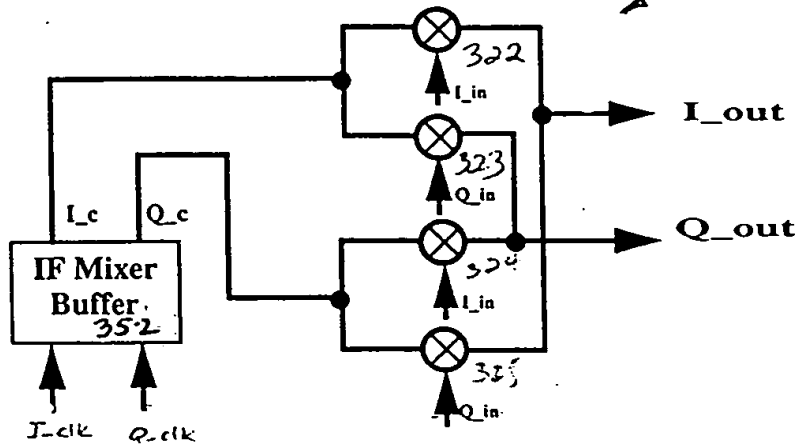


FIG. 17(b)

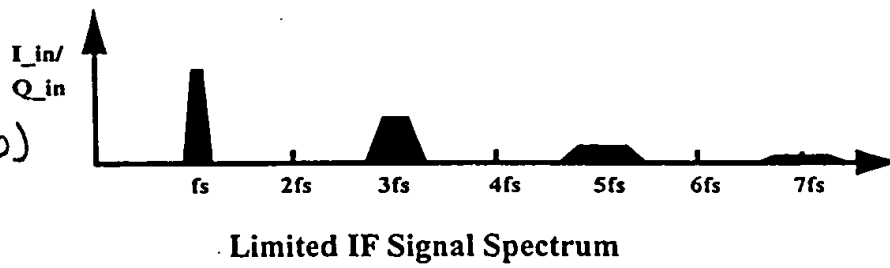


FIG. 17(c)

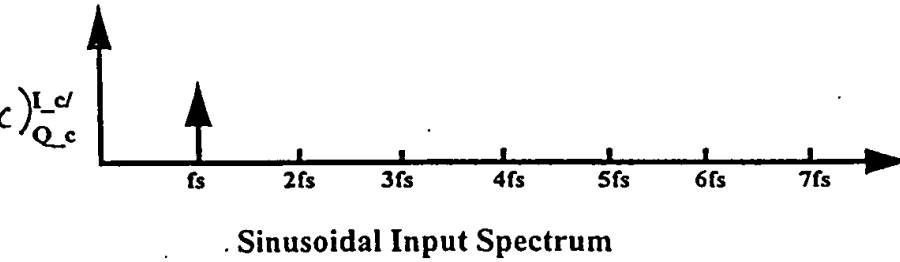


FIG. 17(d)

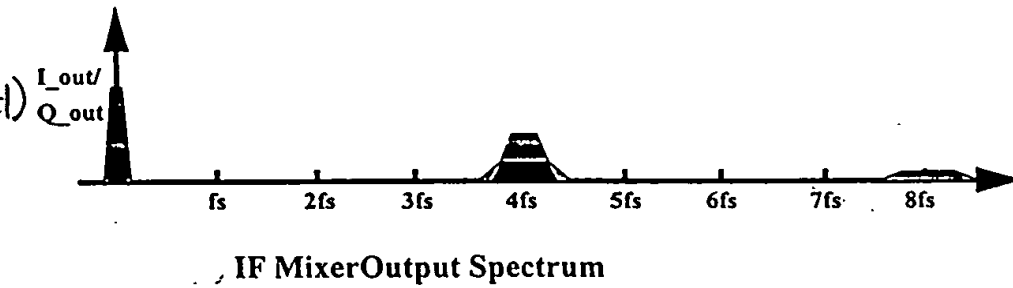


FIG. 18

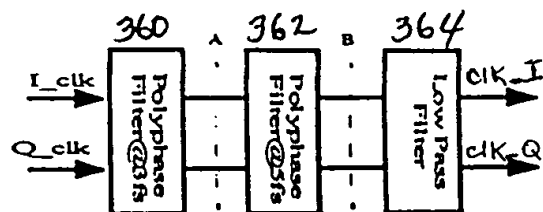


FIG. 19(a)

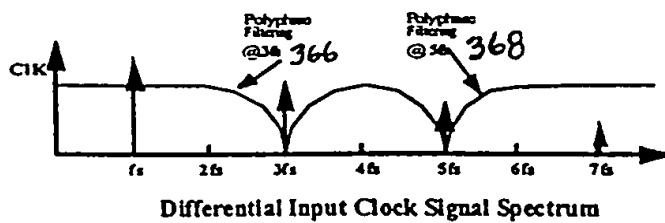


FIG. 19(b)

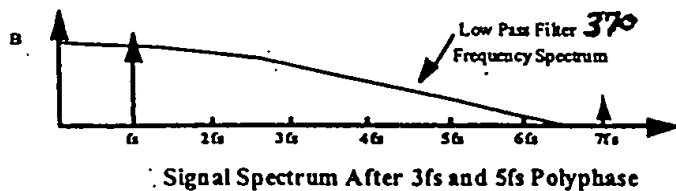


FIG. 19(c)

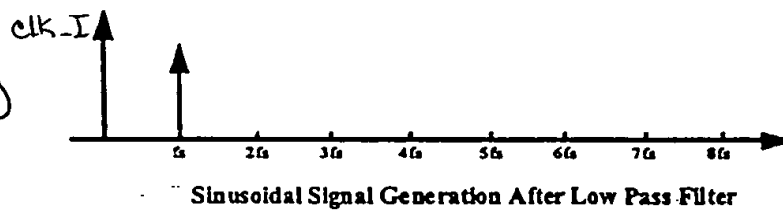


FIG. 19d is a schematic diagram of a circuit 326.

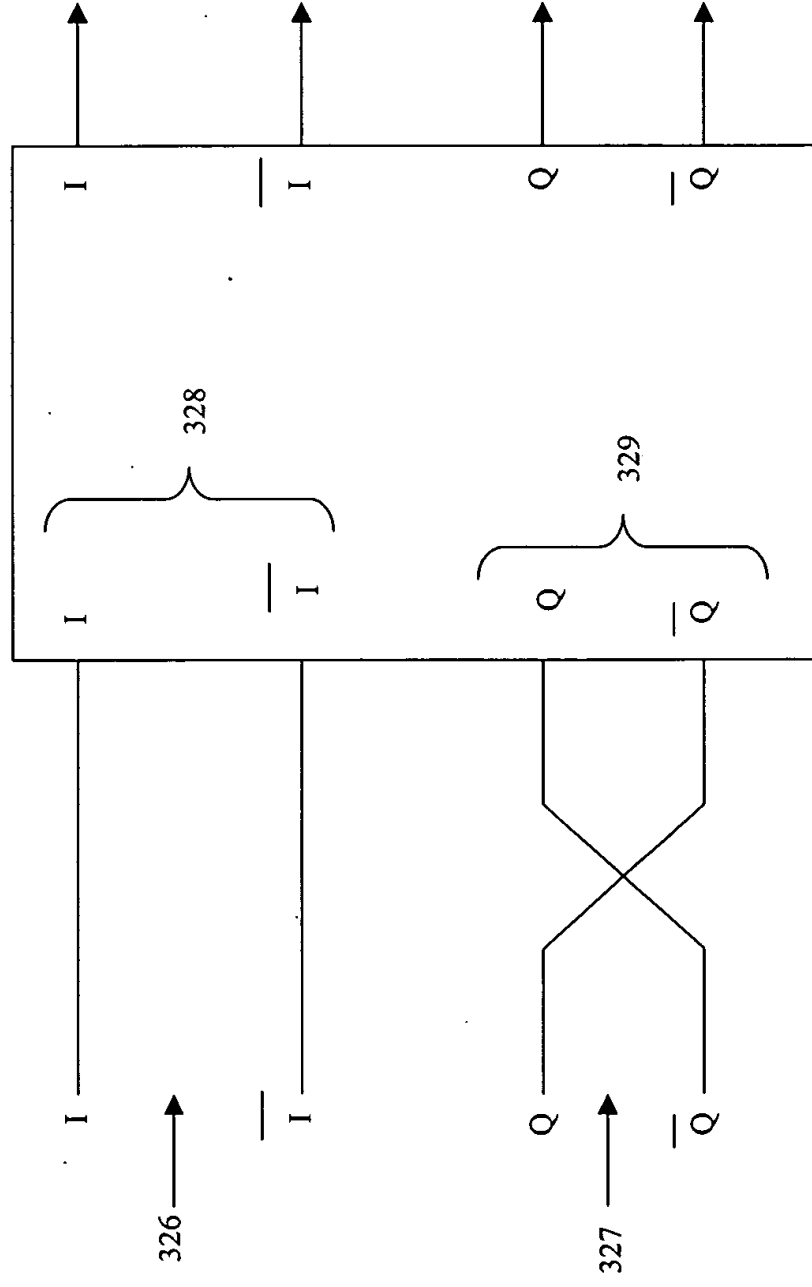


FIG. 19d

FIG. 19e is a schematic diagram of a system 332, which includes two processing units 333 and 334. Each unit has an input I and an output Q. The system 332 is configured to process data in a specific manner, as indicated by the connections between the units.

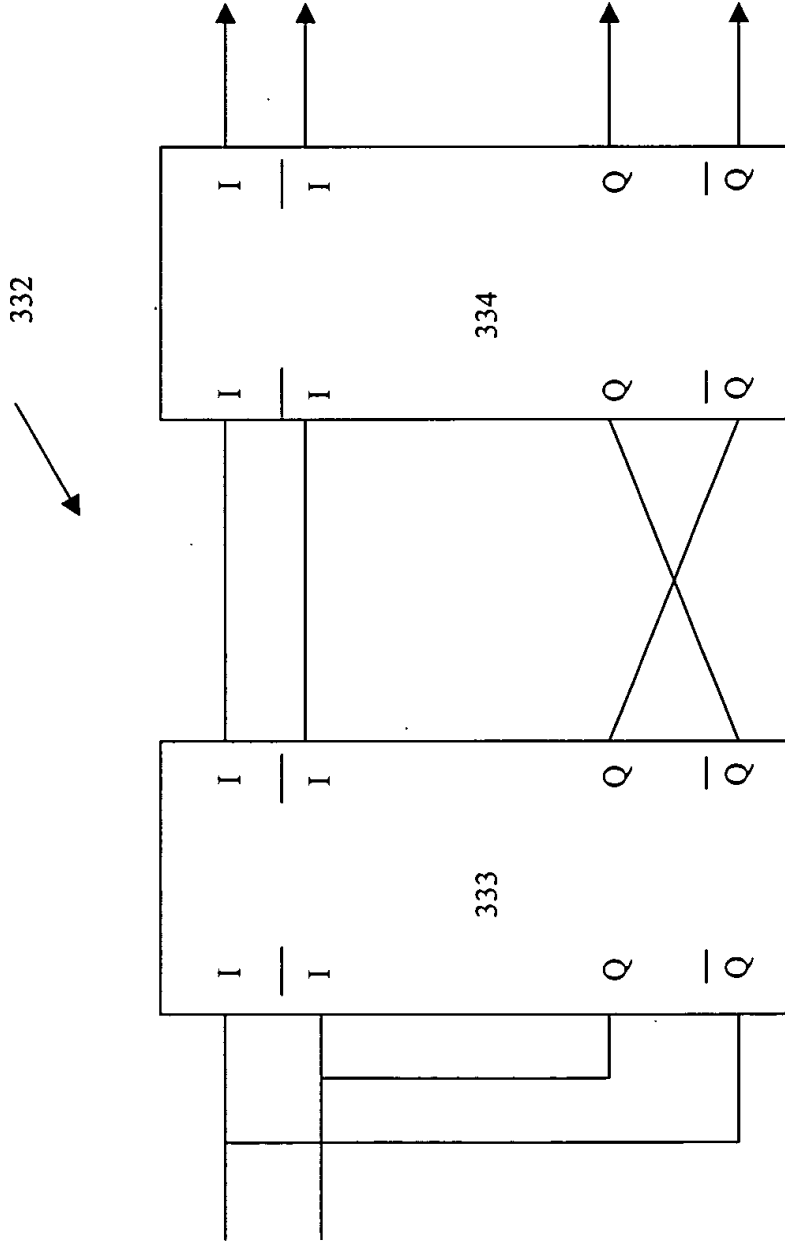


FIG. 19e





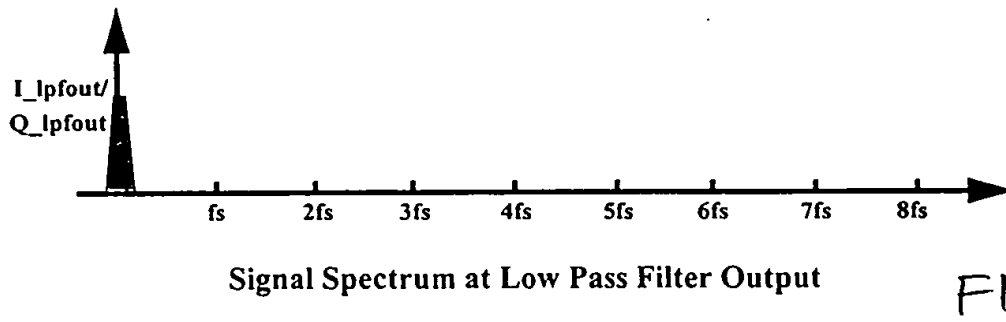
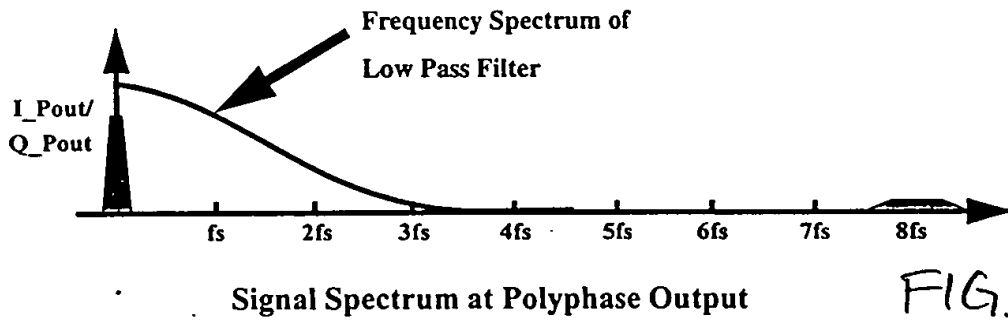
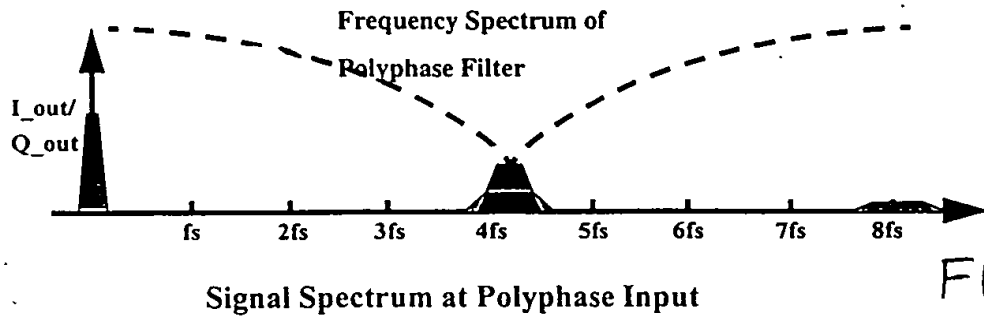




FIG. 21

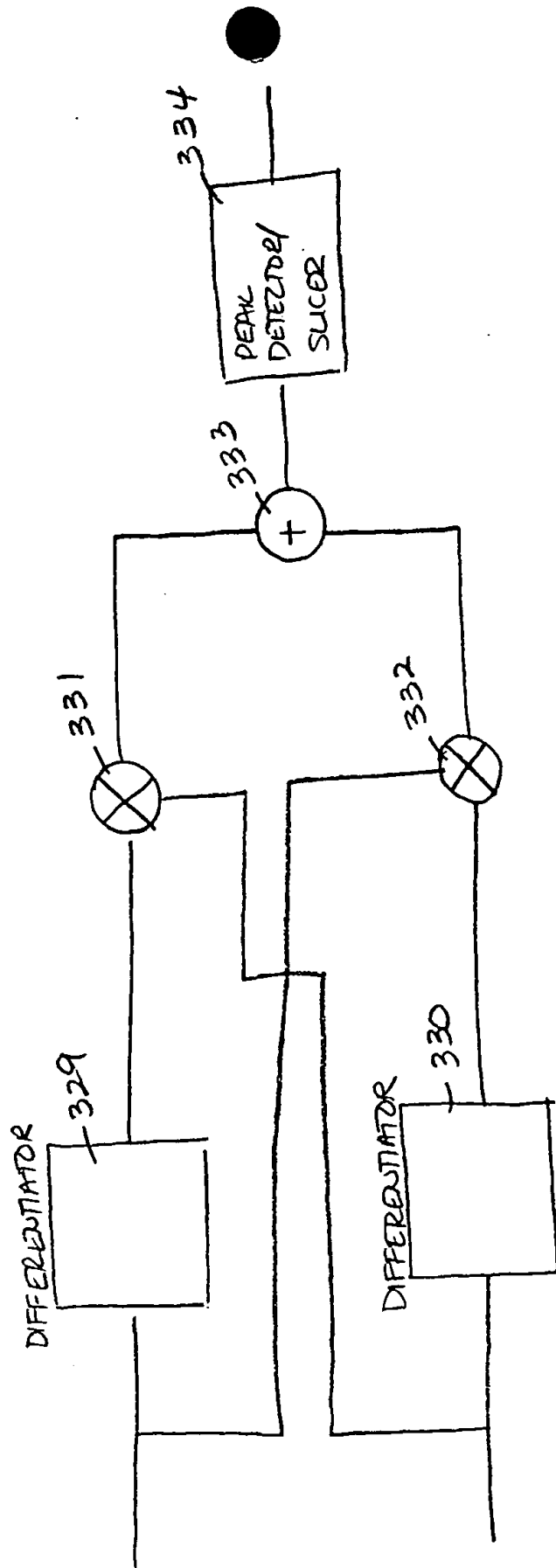


FIG. 21

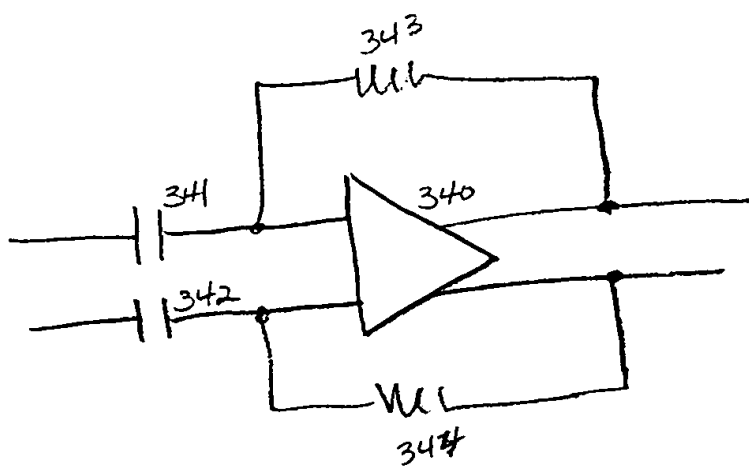


FIGURE 22

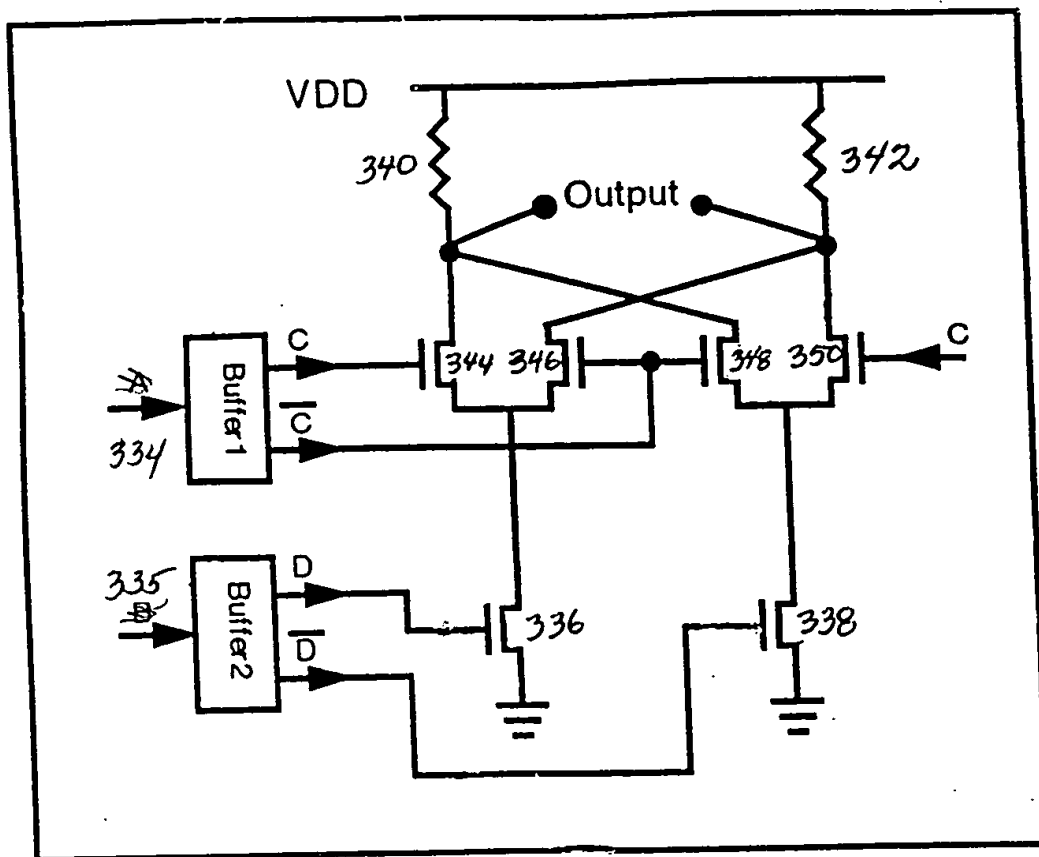


FIG. 23

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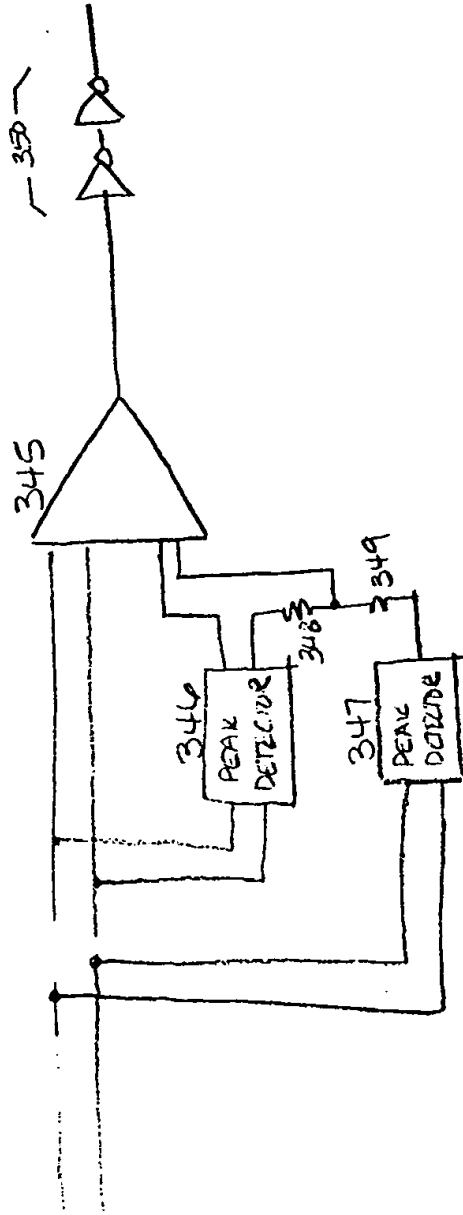


FIGURE 24



FIG. 26(a)

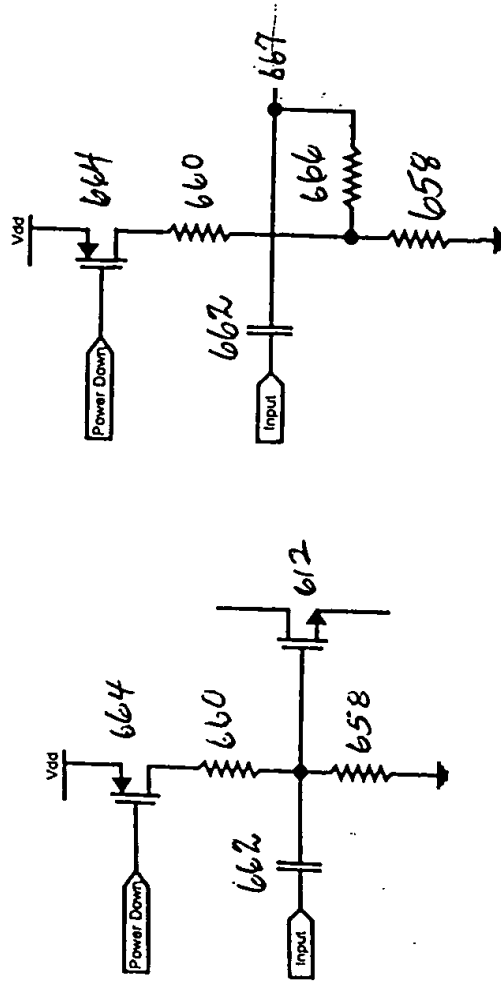


FIG. 26(a)

FIG. 26(b)

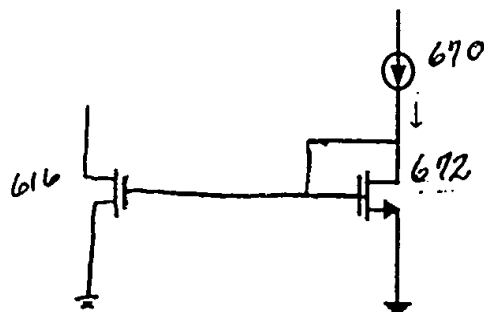


FIG. 27

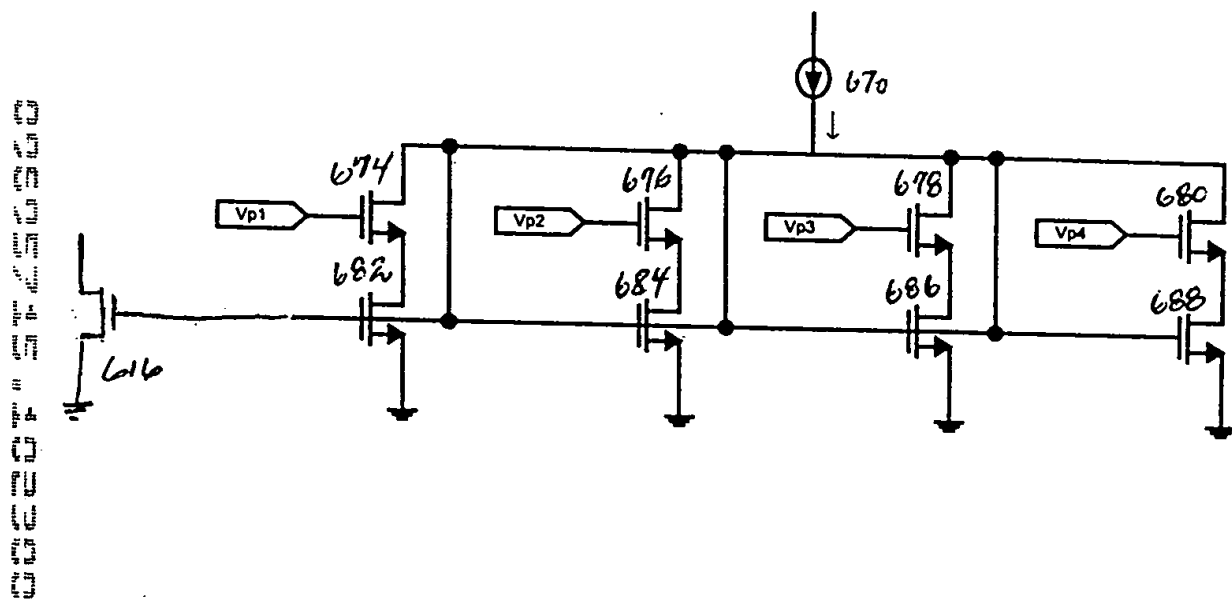


FIG. 28



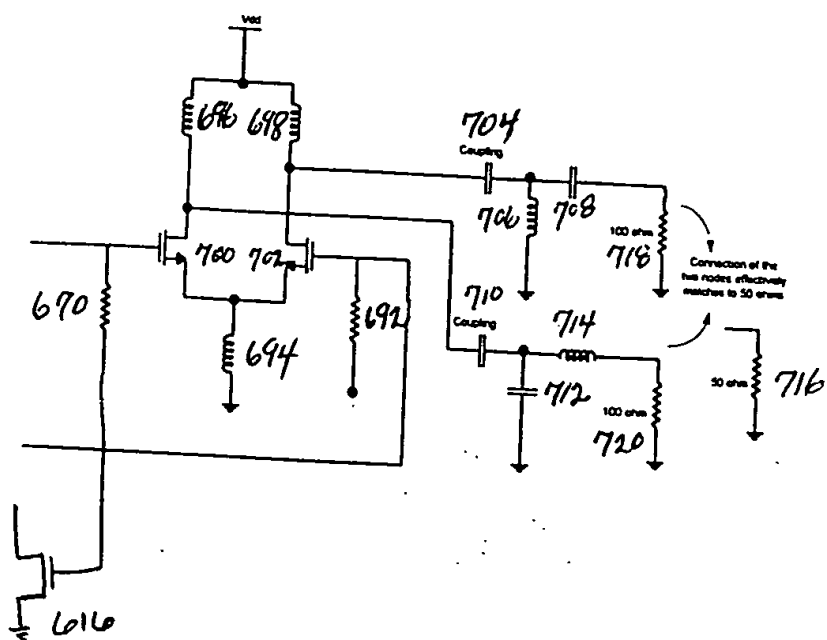


FIG. 29

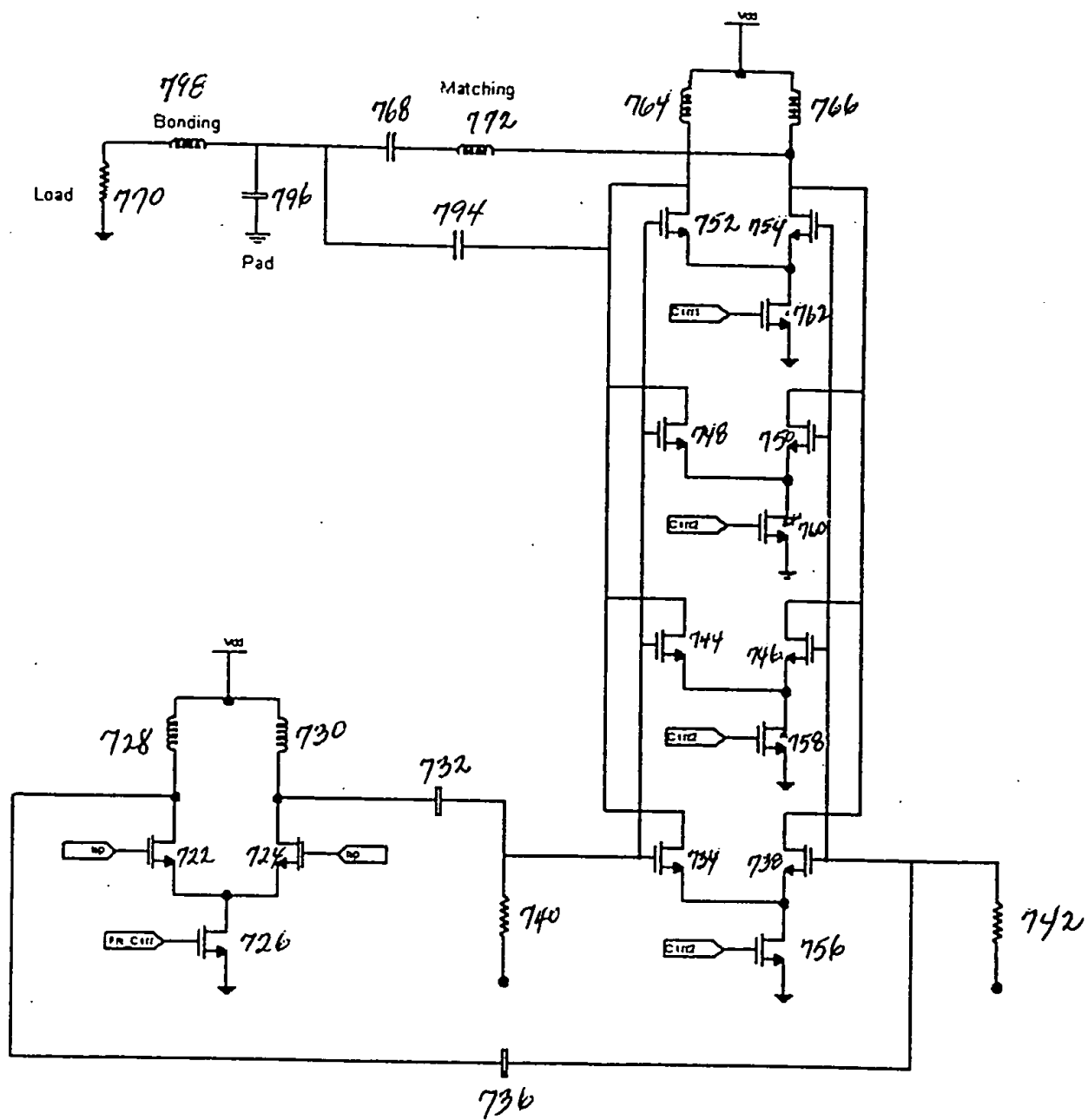


FIG. 30A

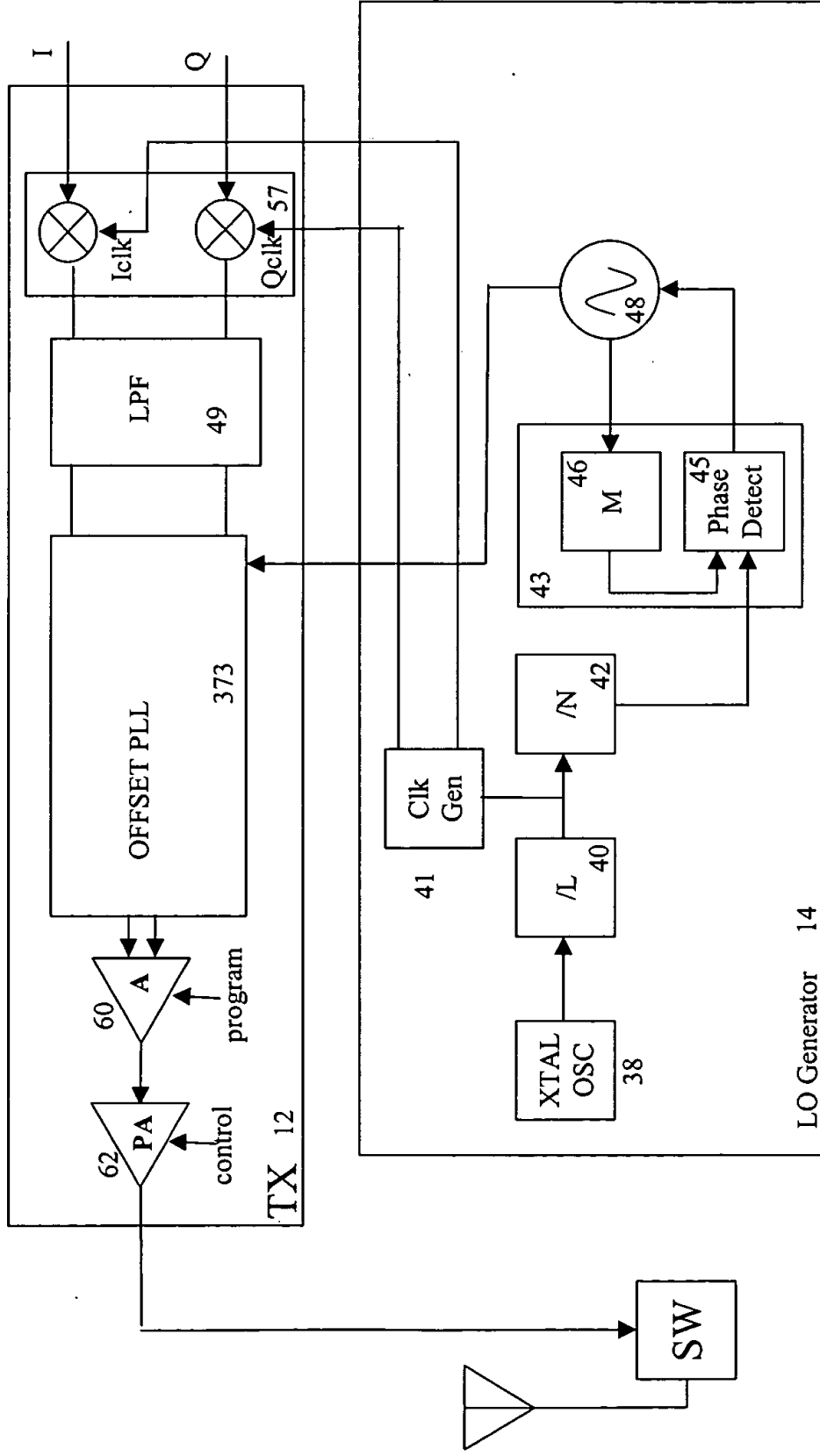


FIG. 30b

US 2003/0126000 A1

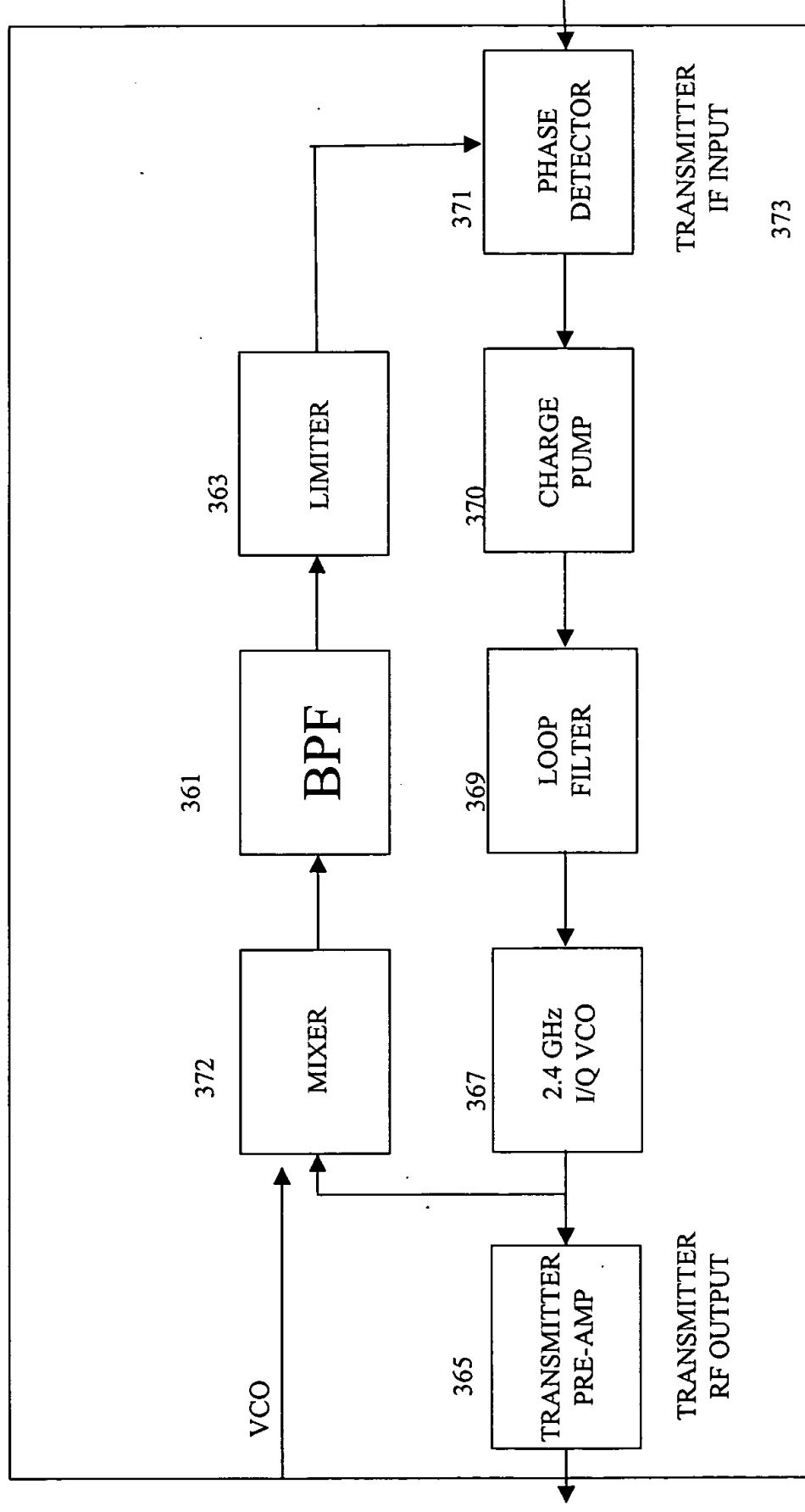
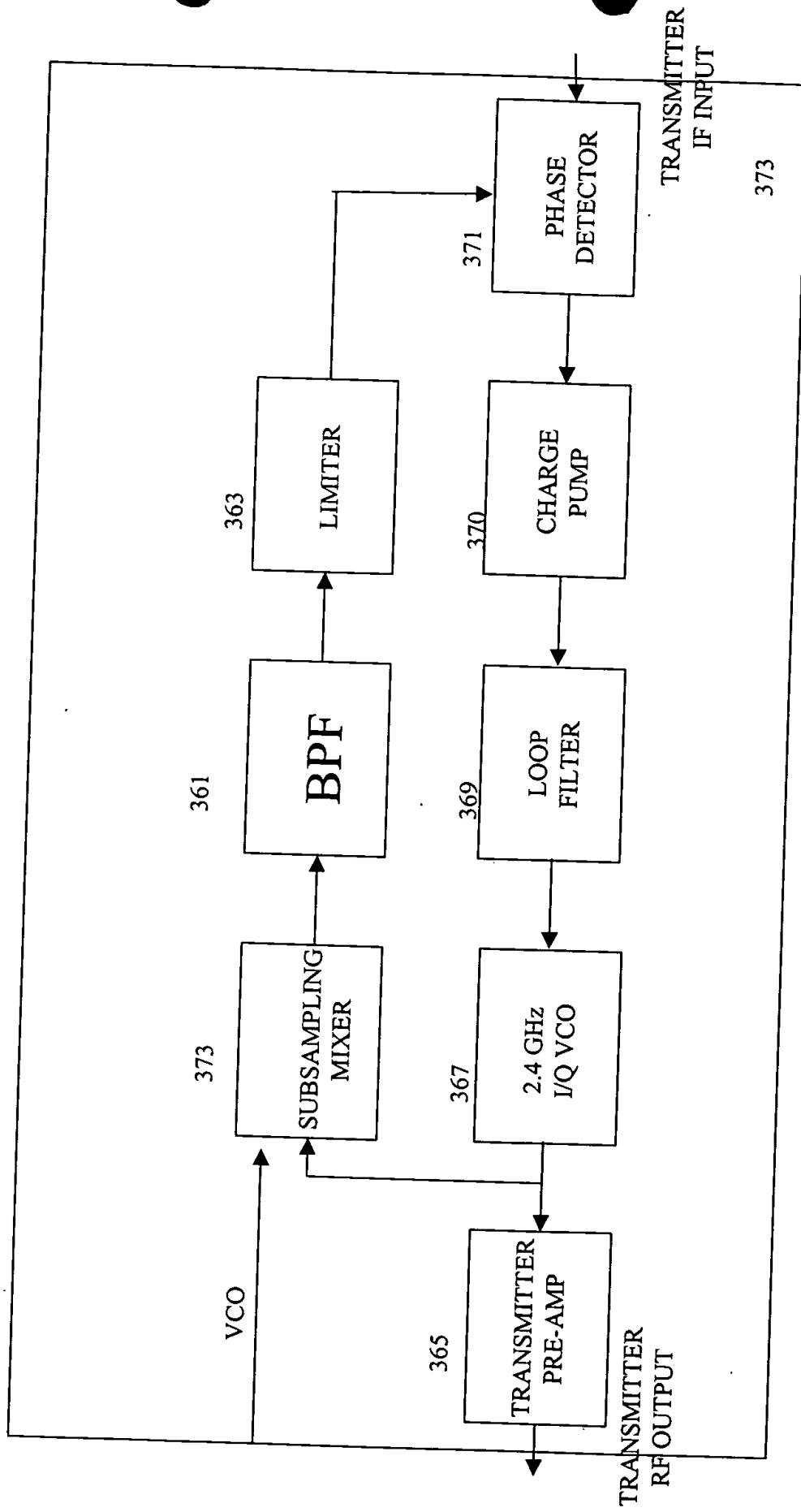


FIG. 30c

US 6,800,000 B2



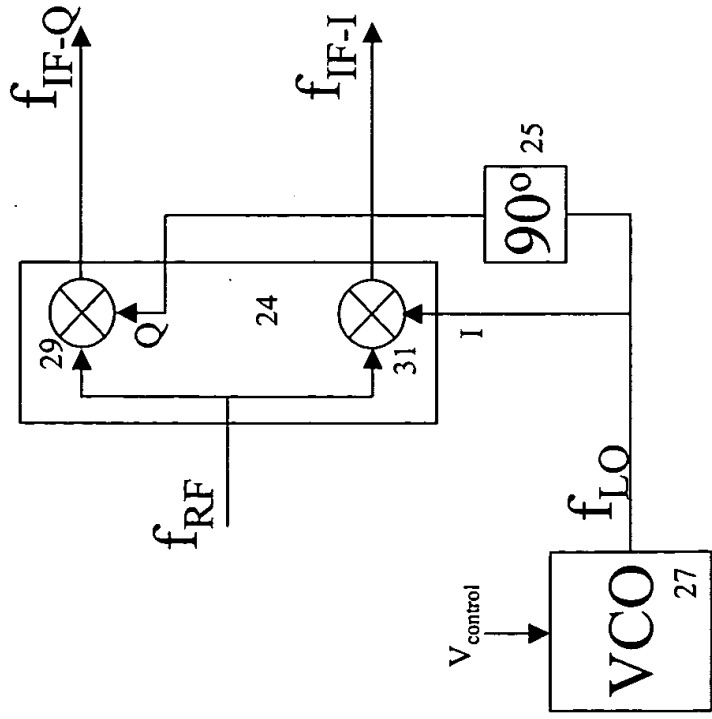


FIG. 30e

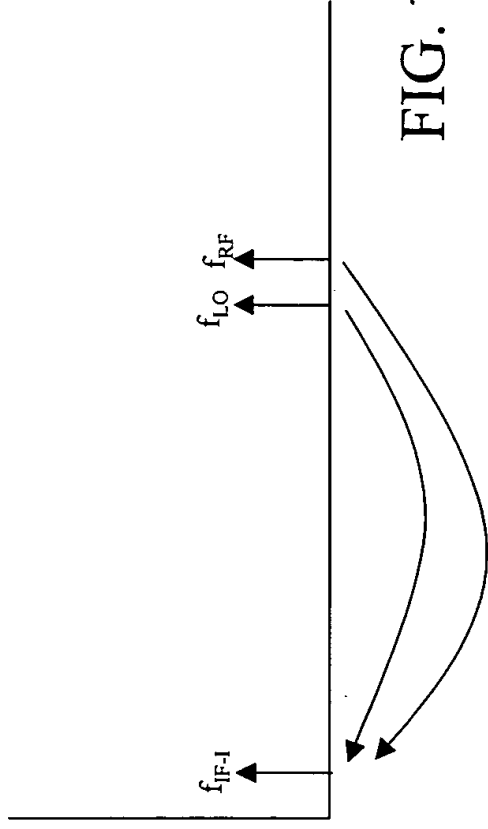


FIG. 30f

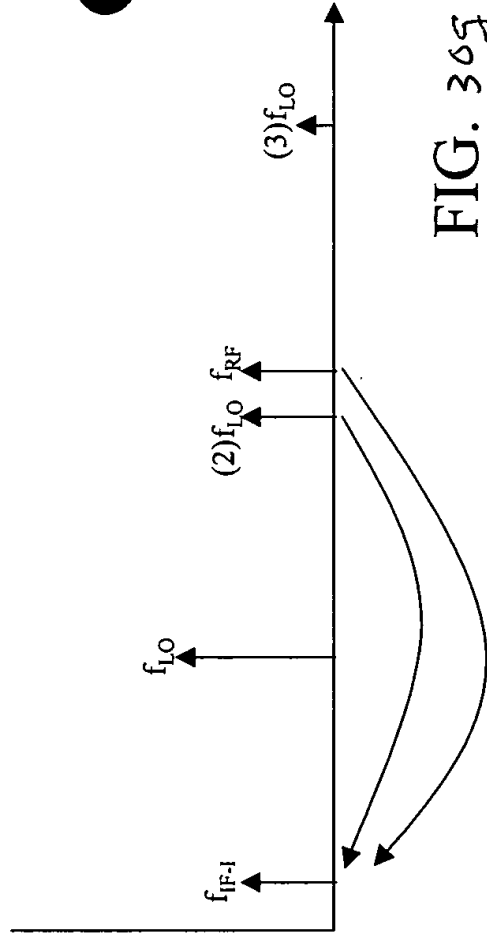


FIG. 30g

FIG. 30A

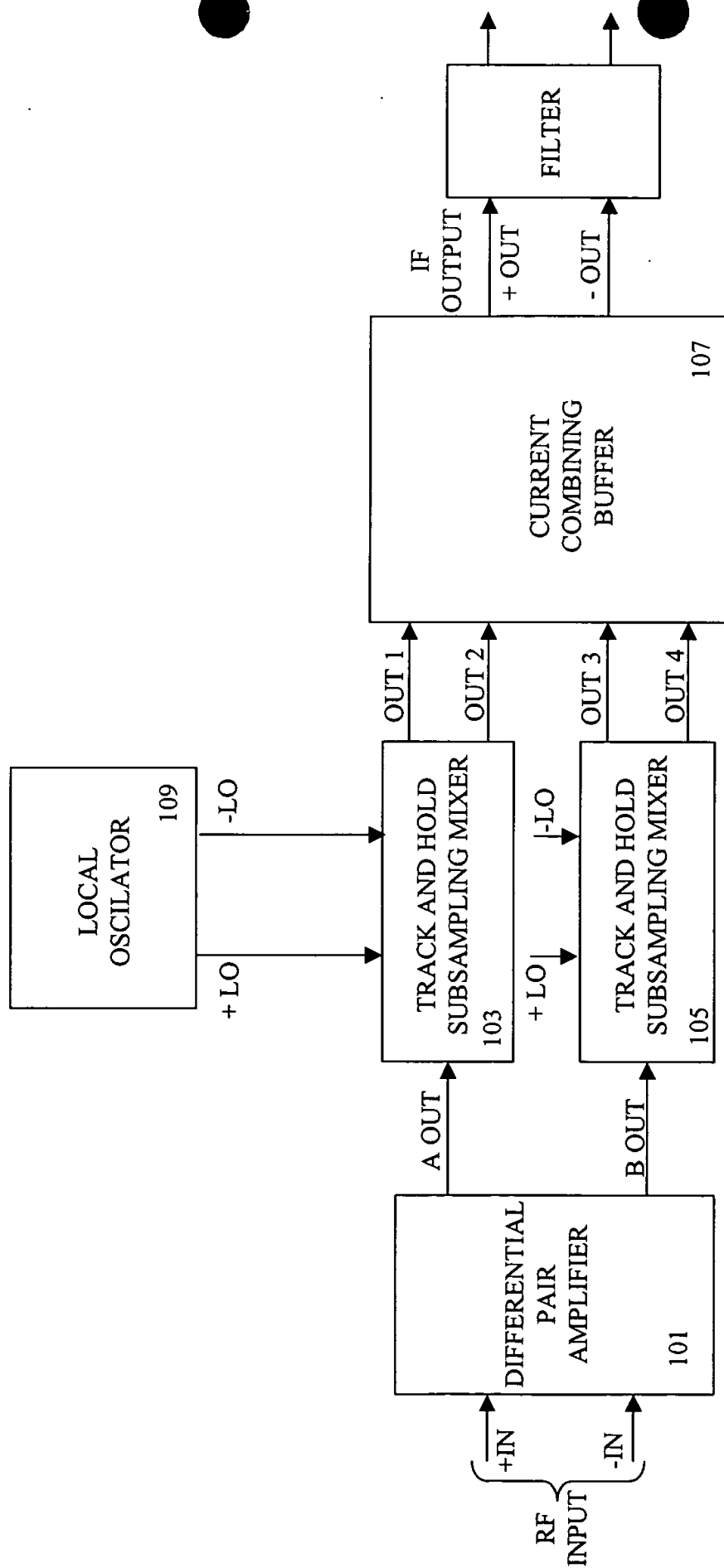


FIG. 30A

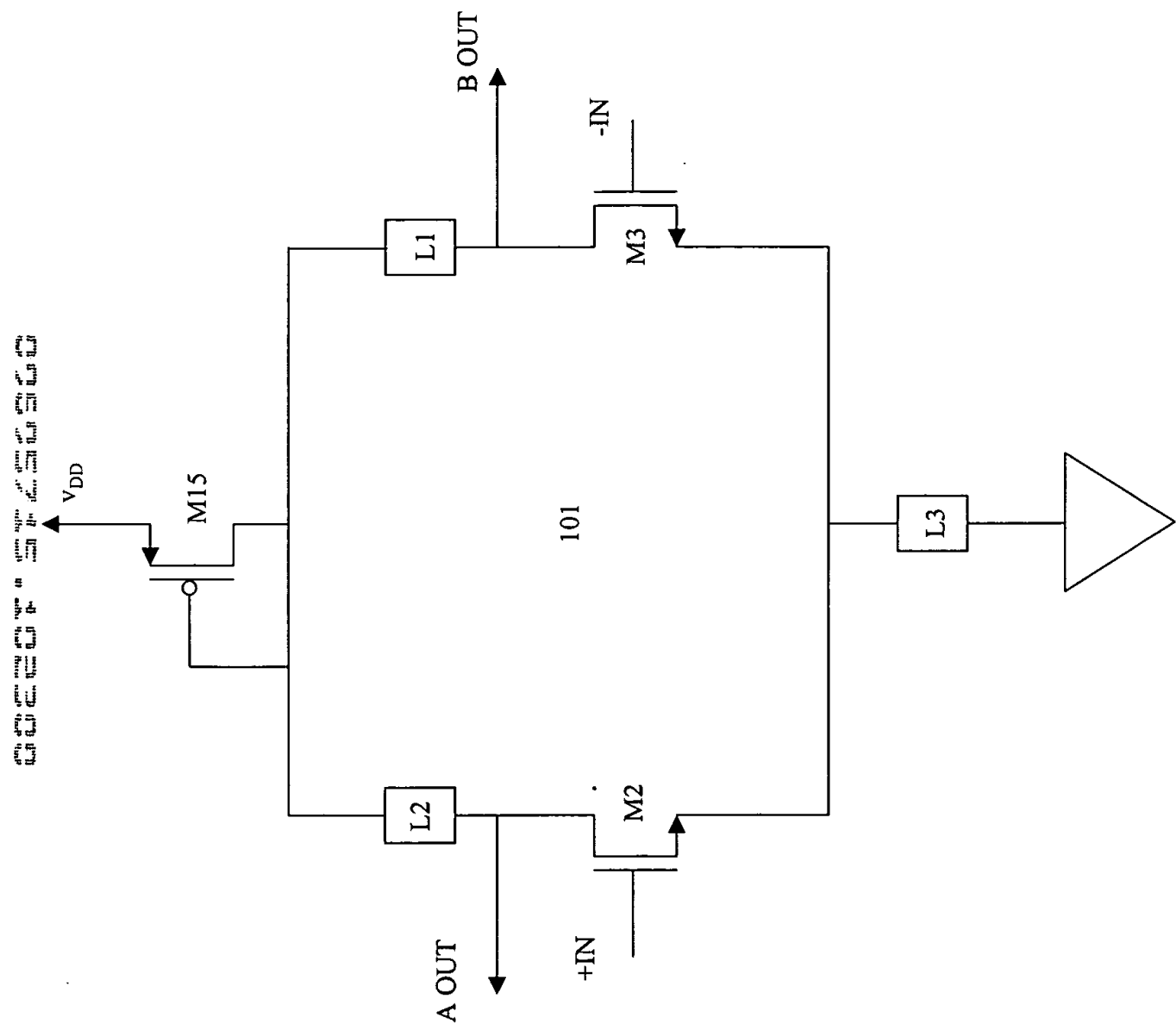


FIG. 30a



FIG. 30j

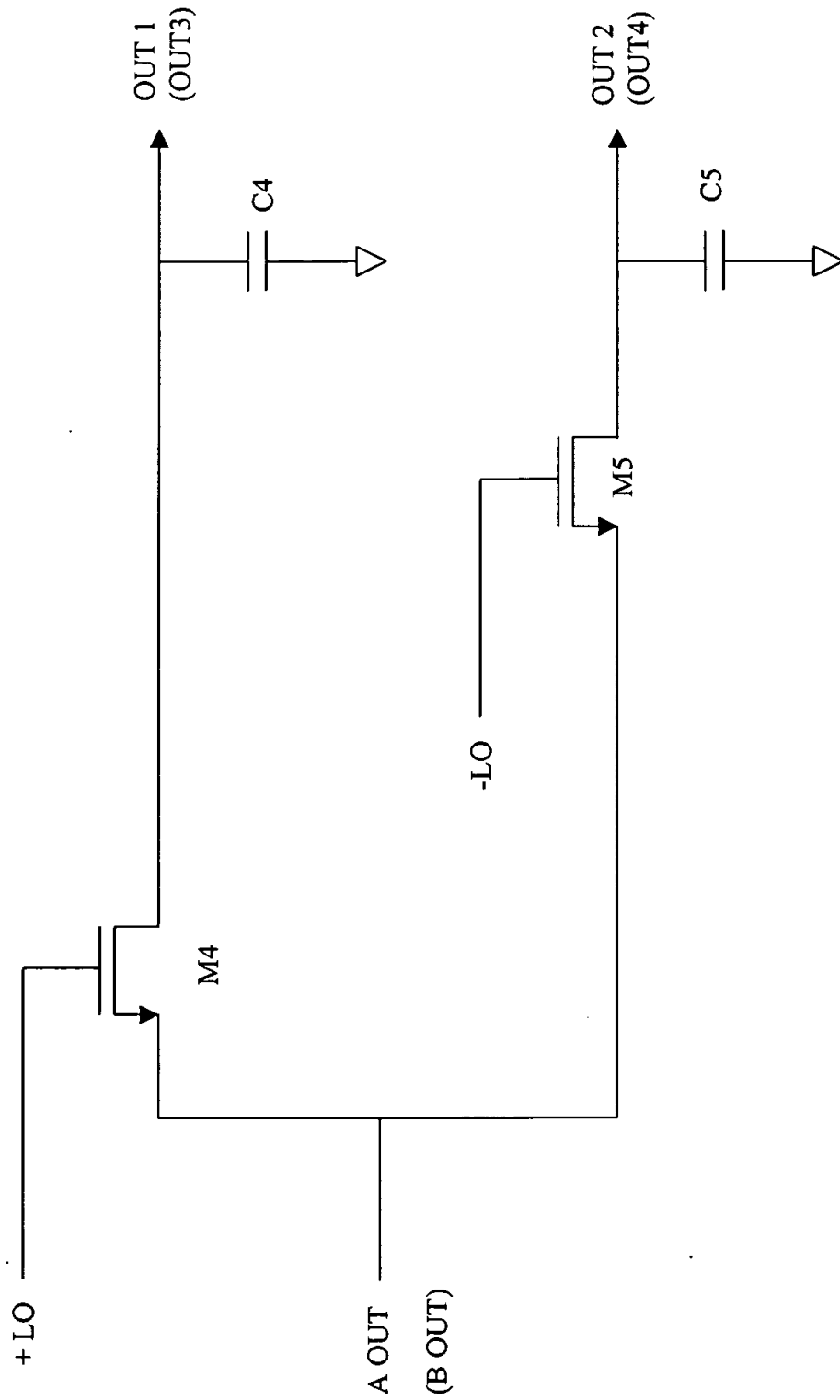


FIG. 30j

FIG. 30k

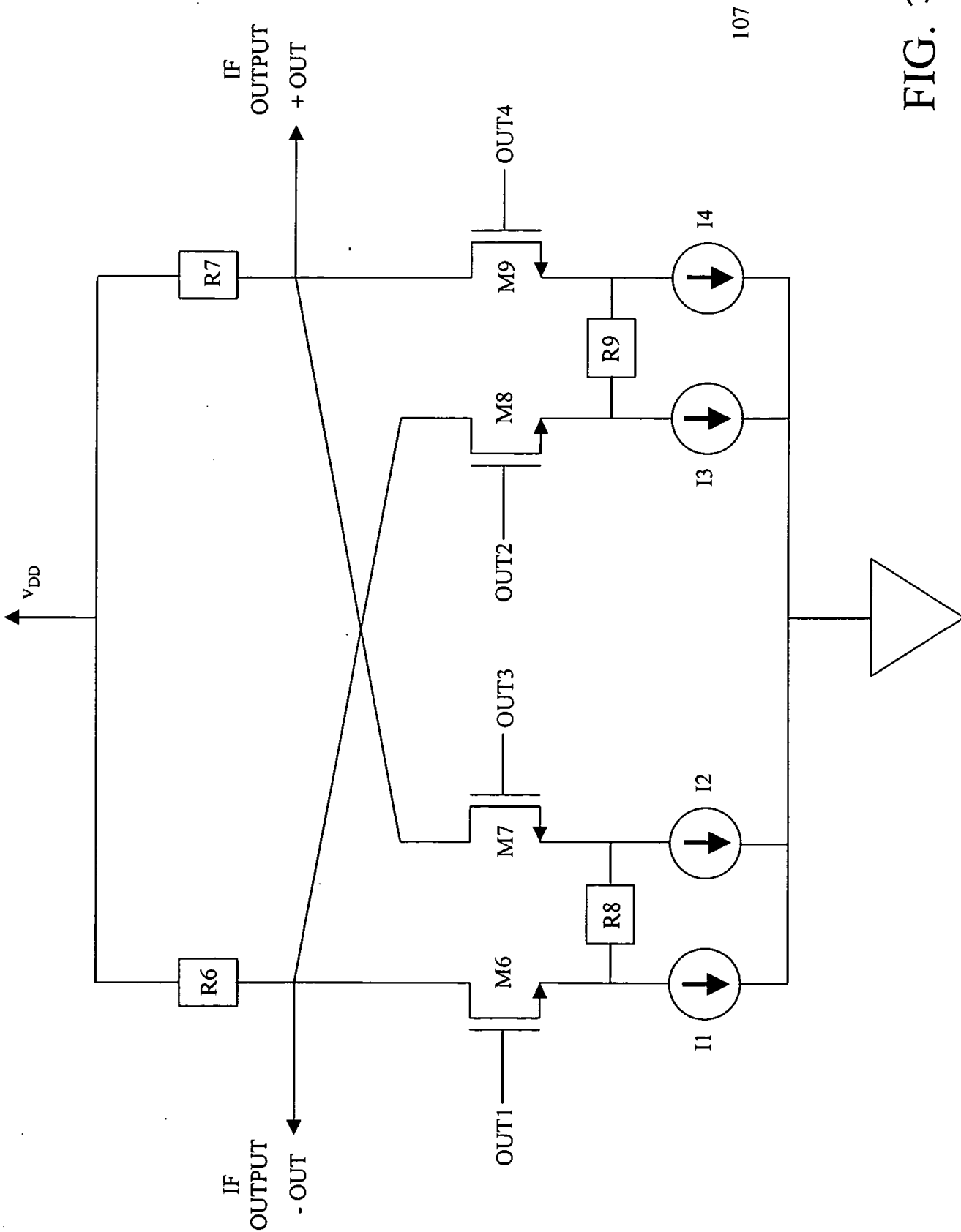


FIG. 30k

FIG. 30L

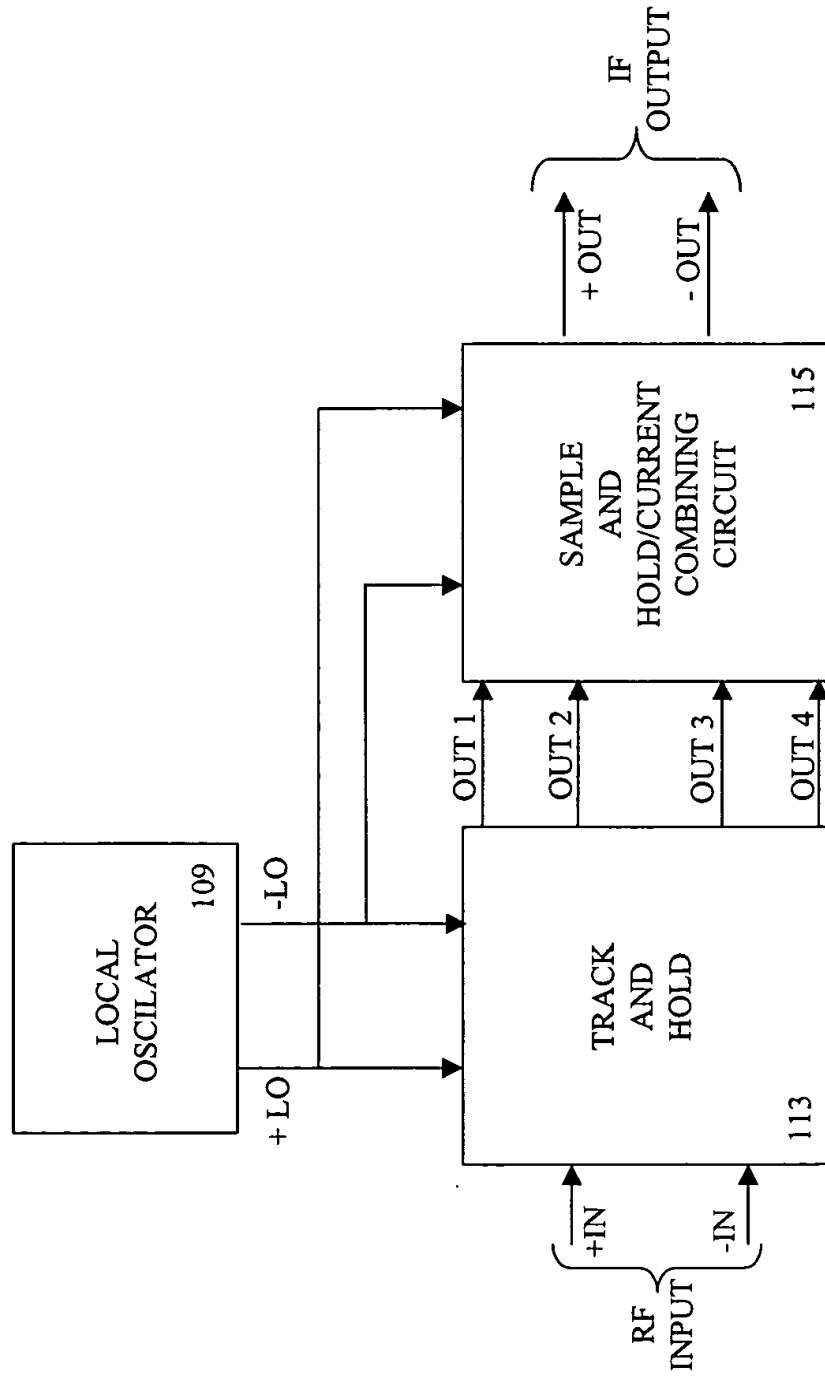
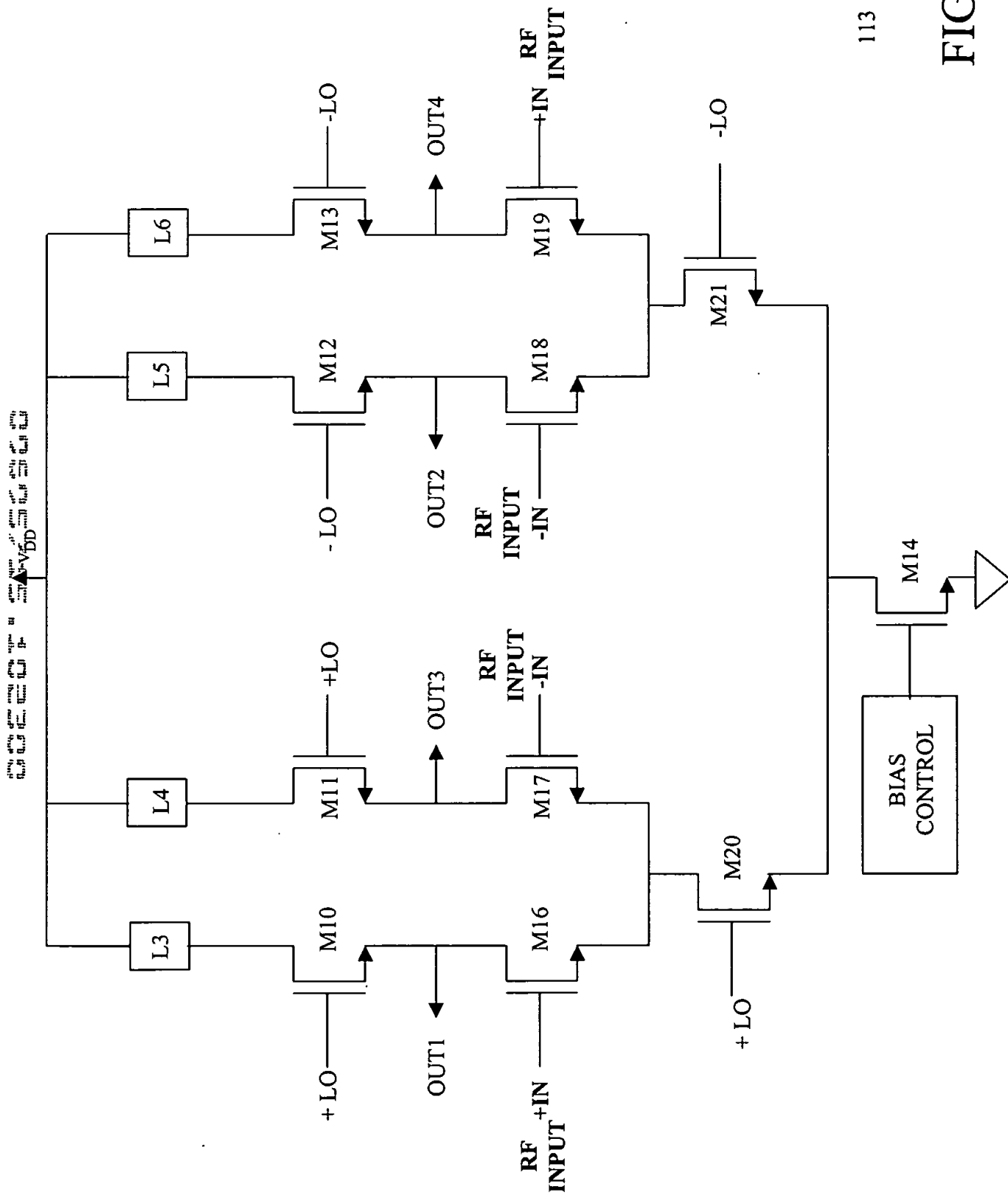


FIG. 30L



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FIG. 30.m

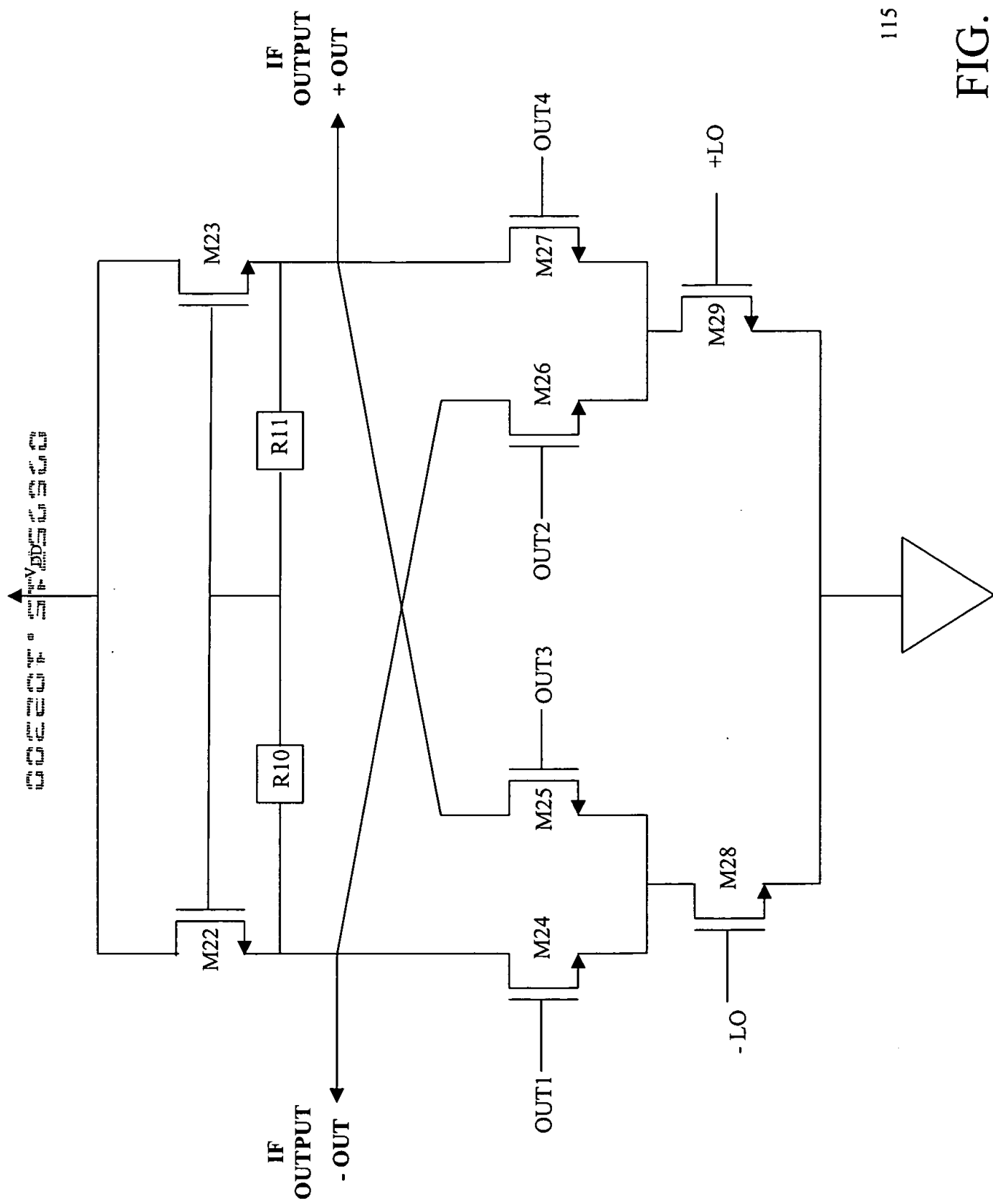


FIG. 30W

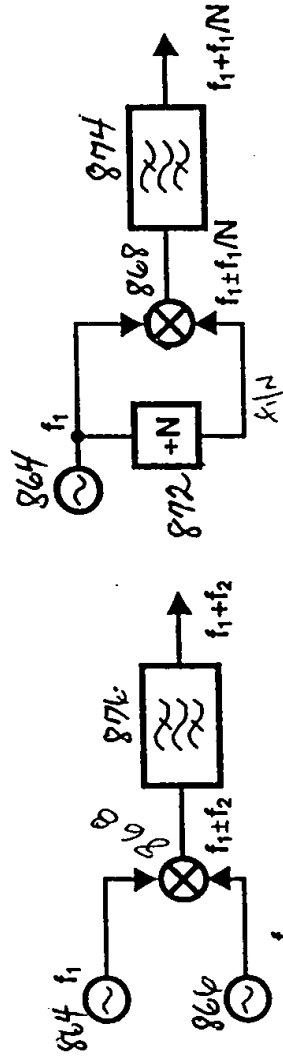


FIG. 31(a)

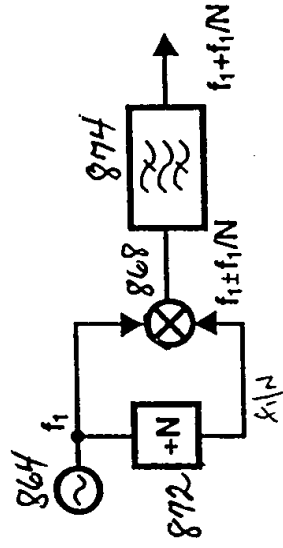


FIG. 31(b)



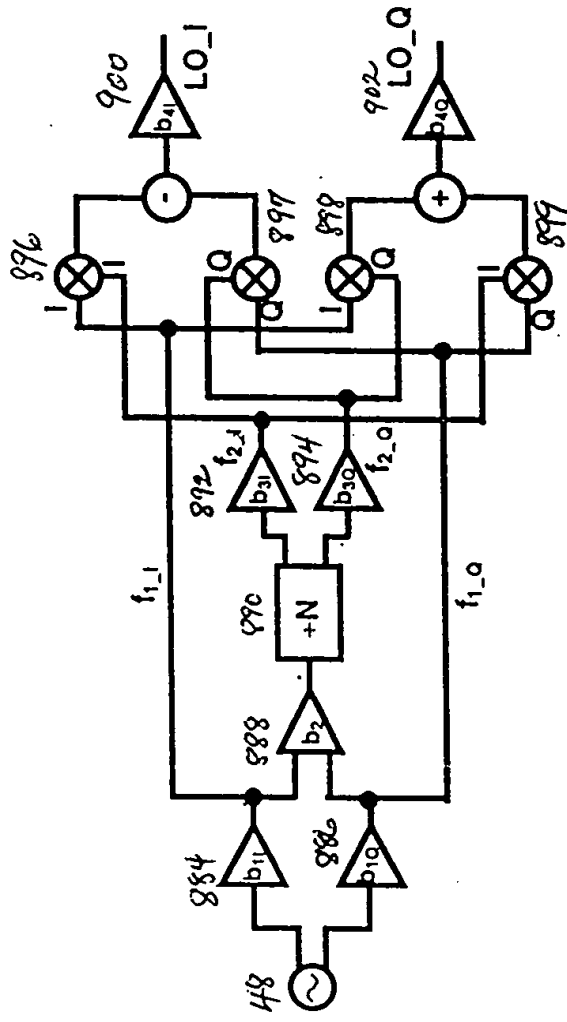


FIG. 33(a)



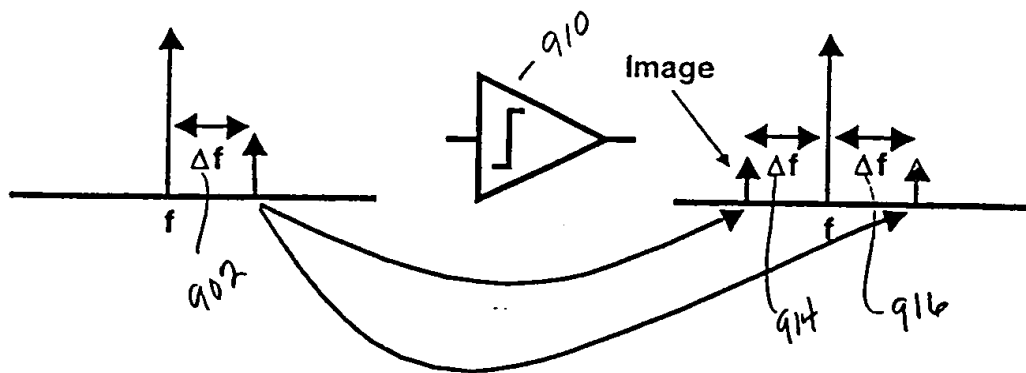


FIG. 33(b)

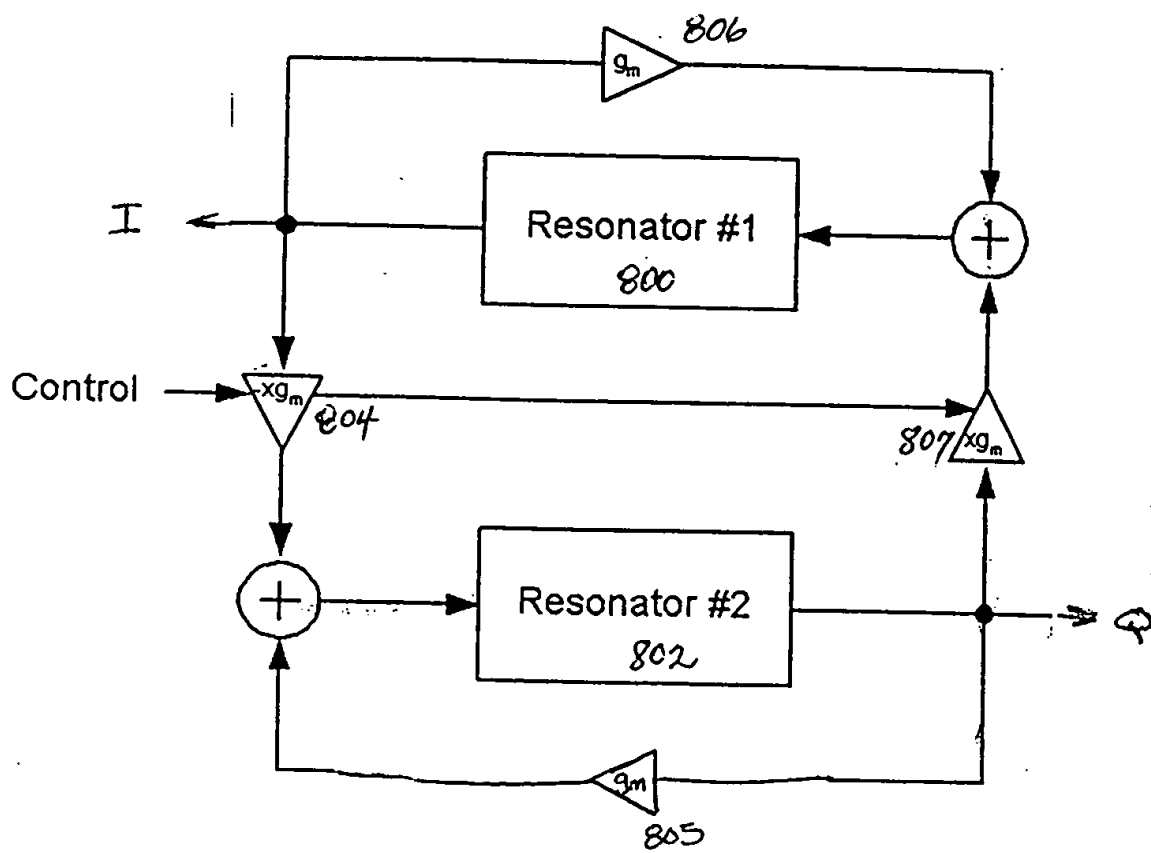


FIG. 34



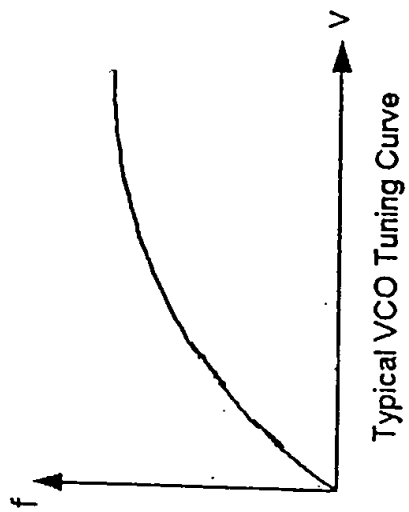


FIG. 36(a)

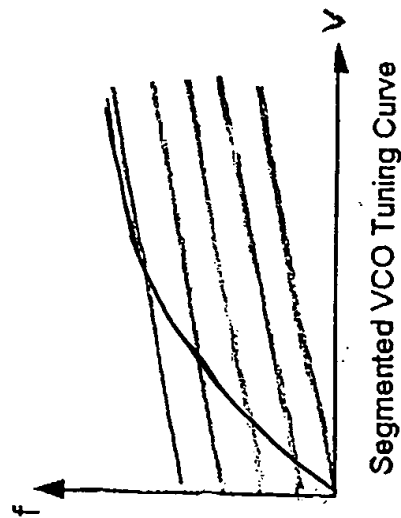


FIG. 36(b)

FIG. 37(a)

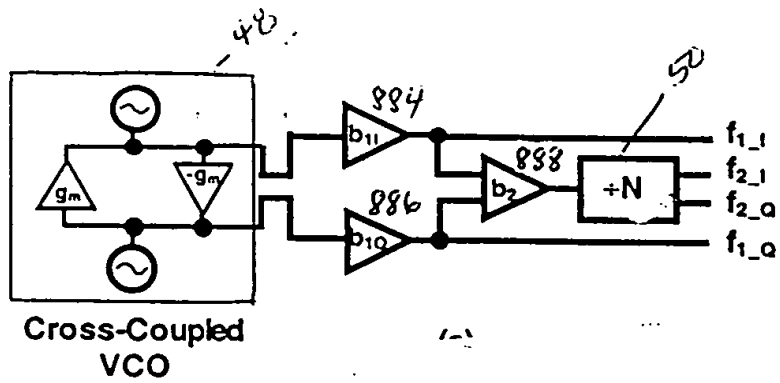
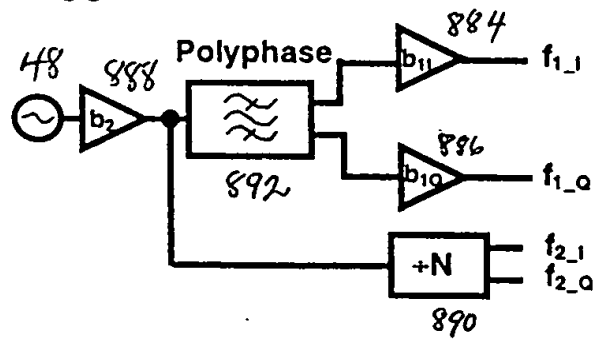
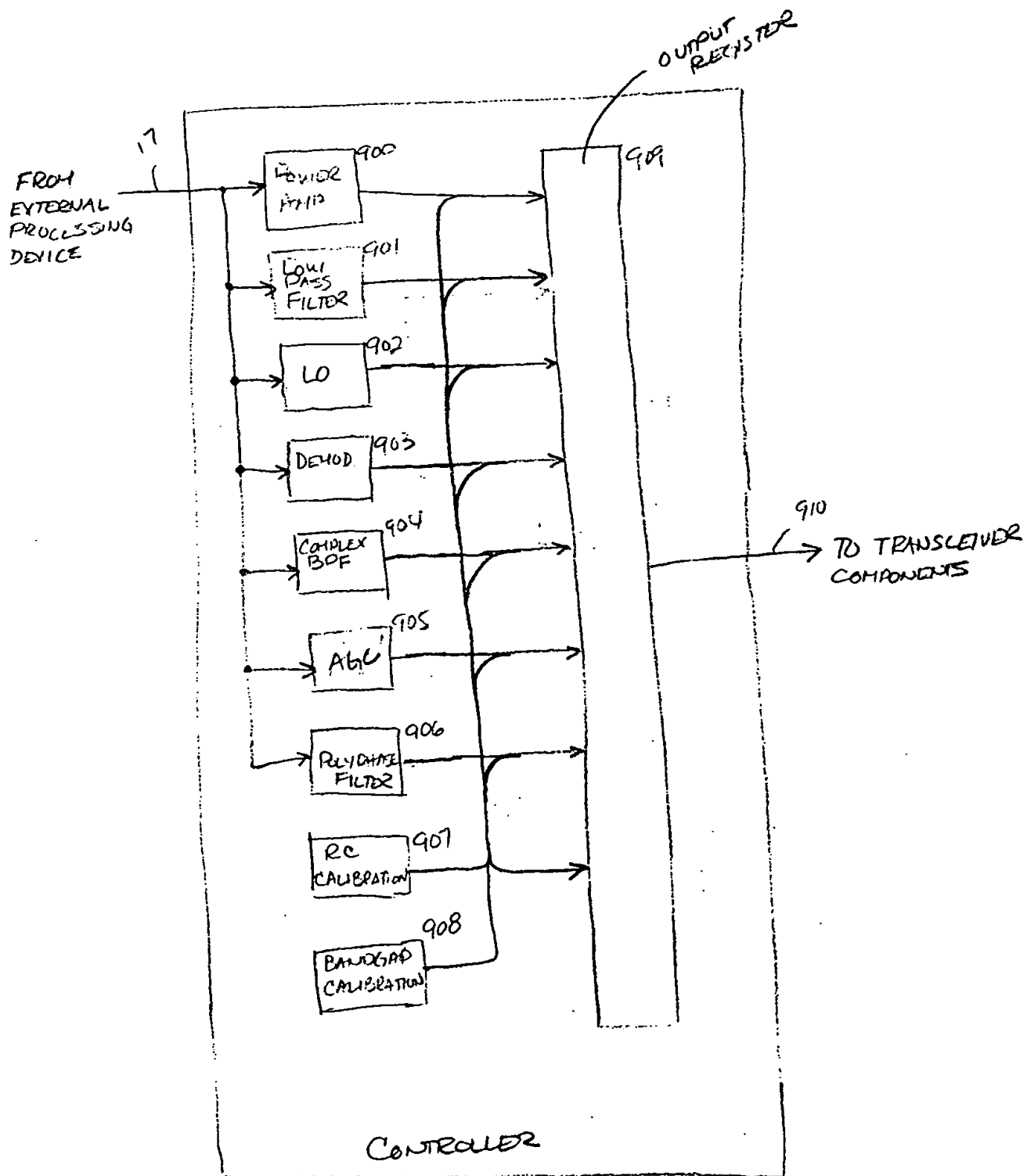


FIG. 37(b)



COMMUNICATIONS





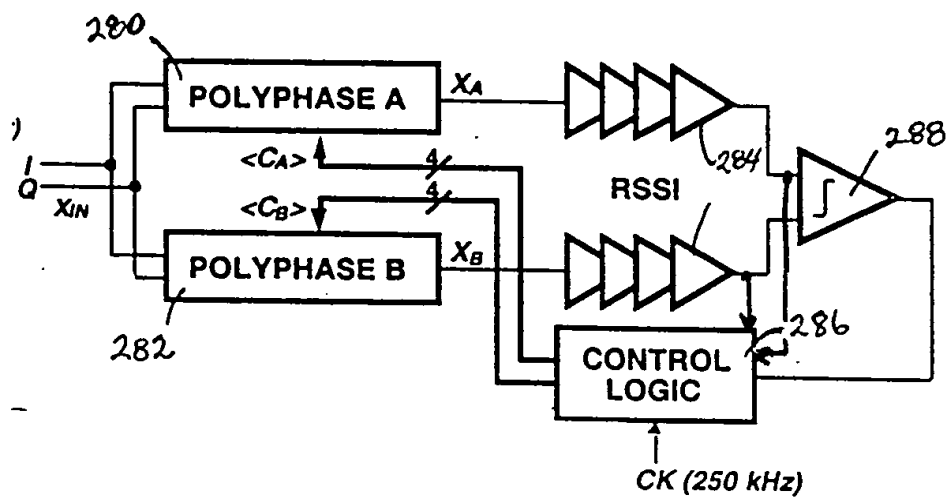


FIG. 40



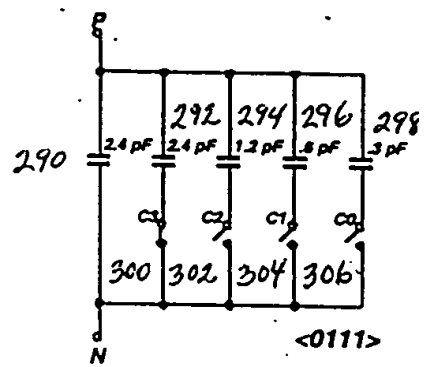


FIG. 41

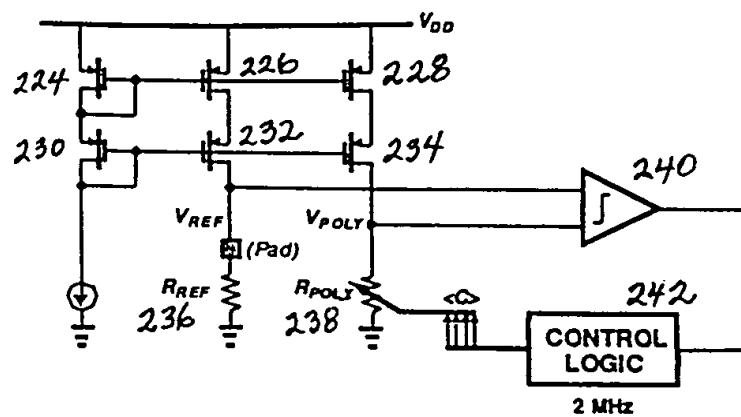


FIG. 42

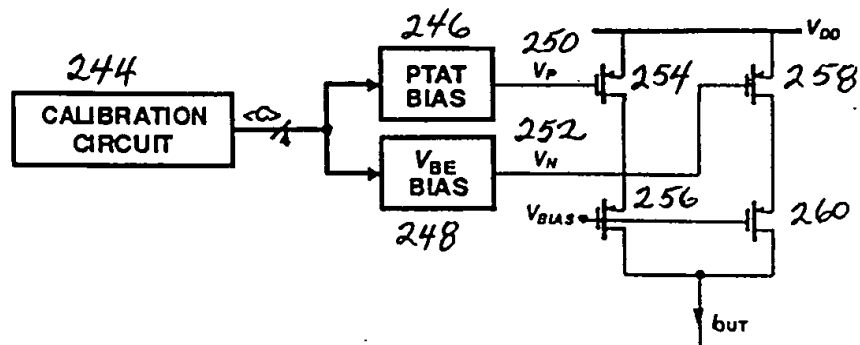


FIG. 43

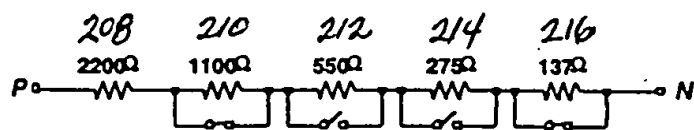


FIG. 44



FIG. 46 is a schematic diagram of a circuit for a radio receiver, showing a tuned circuit, a detector, and an LNA (Low Noise Amplifier) stage.

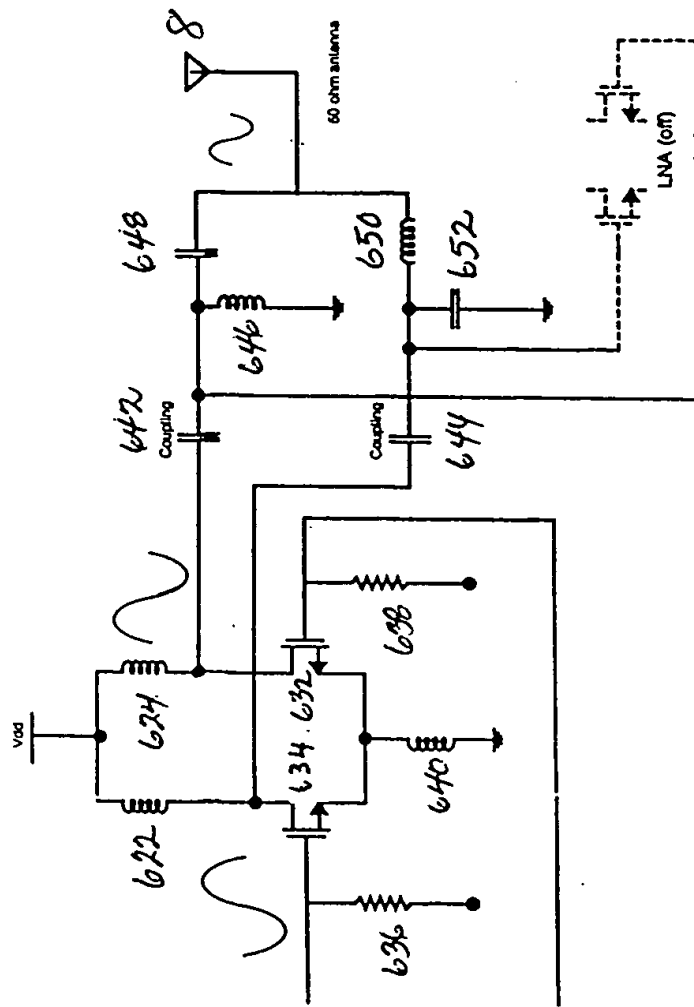


FIG. 46

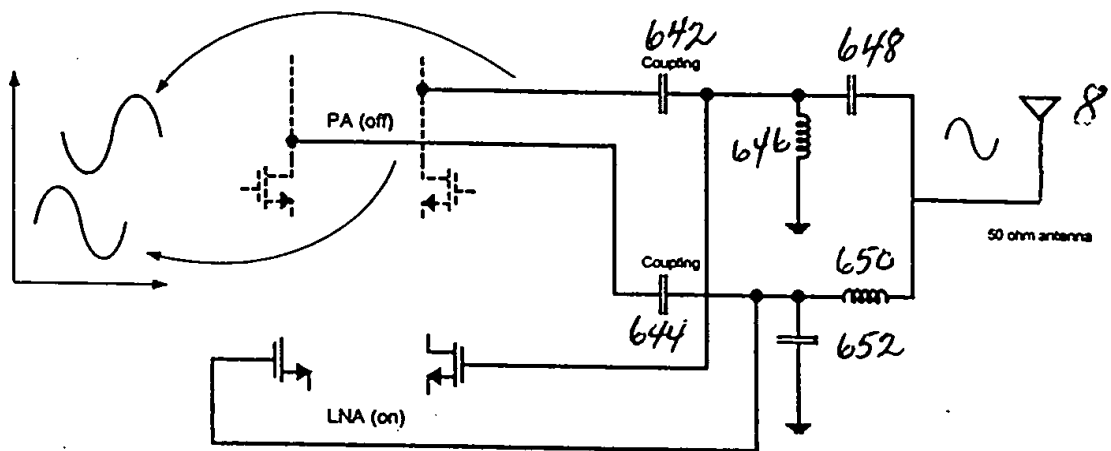


FIG. 47

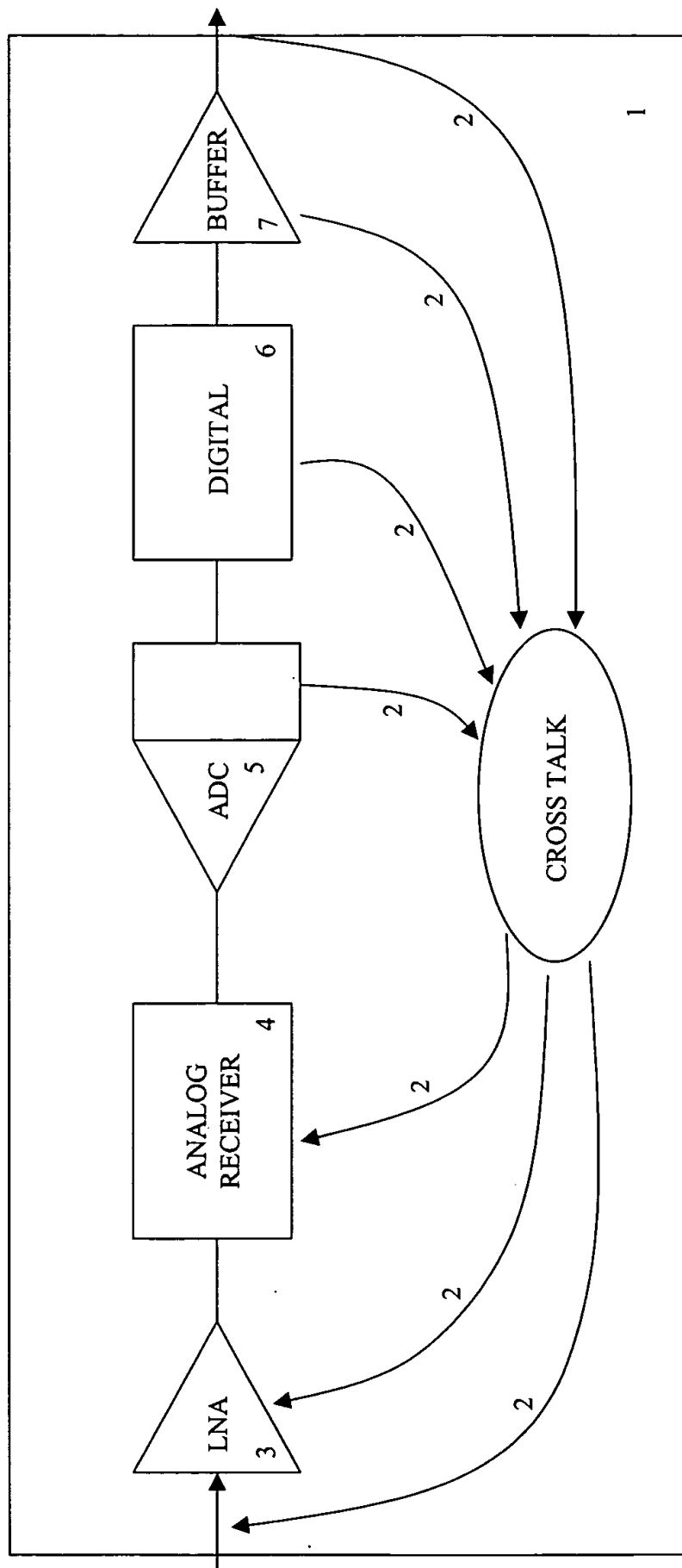


FIG. 48a



FIG. 406

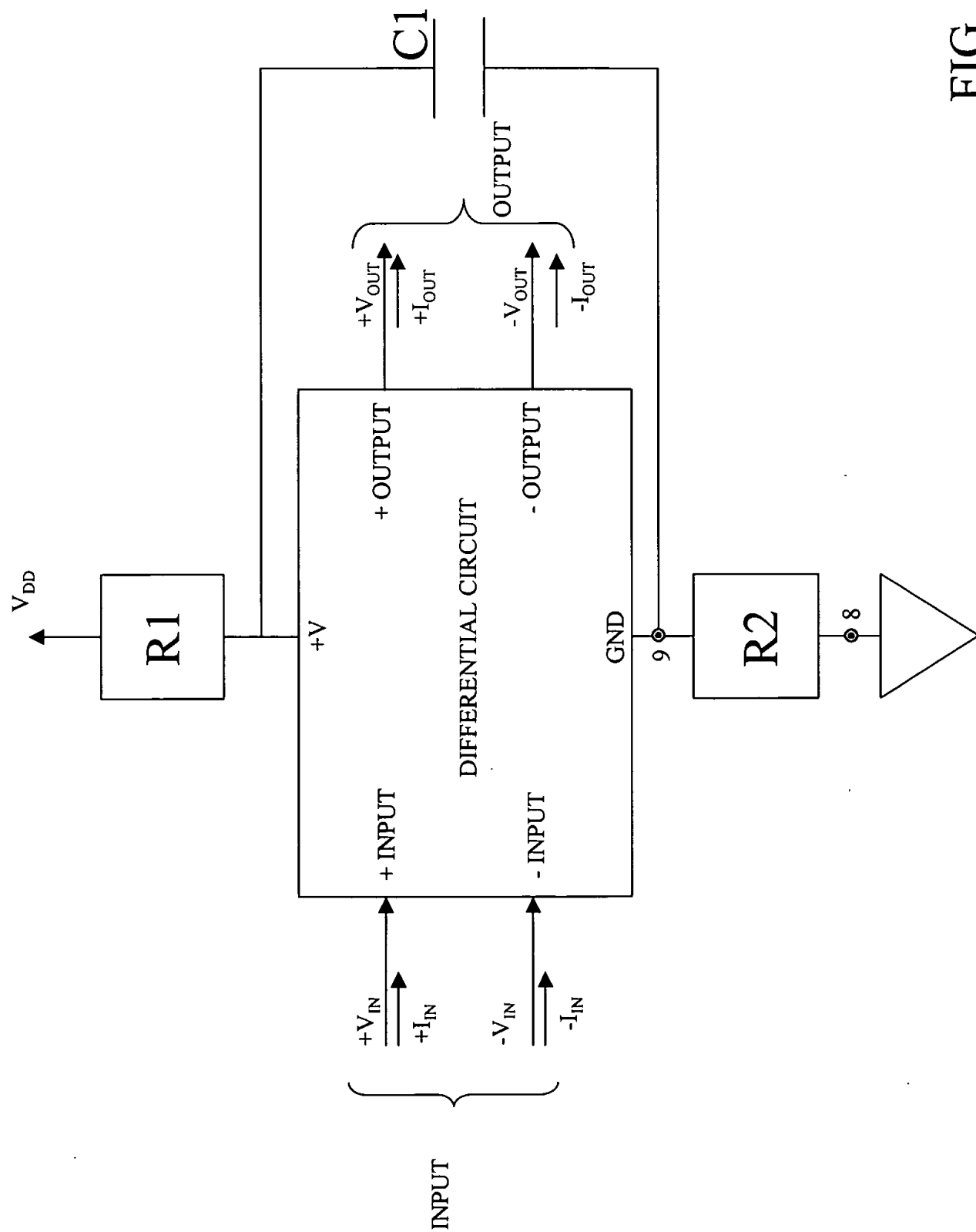


FIG. 406

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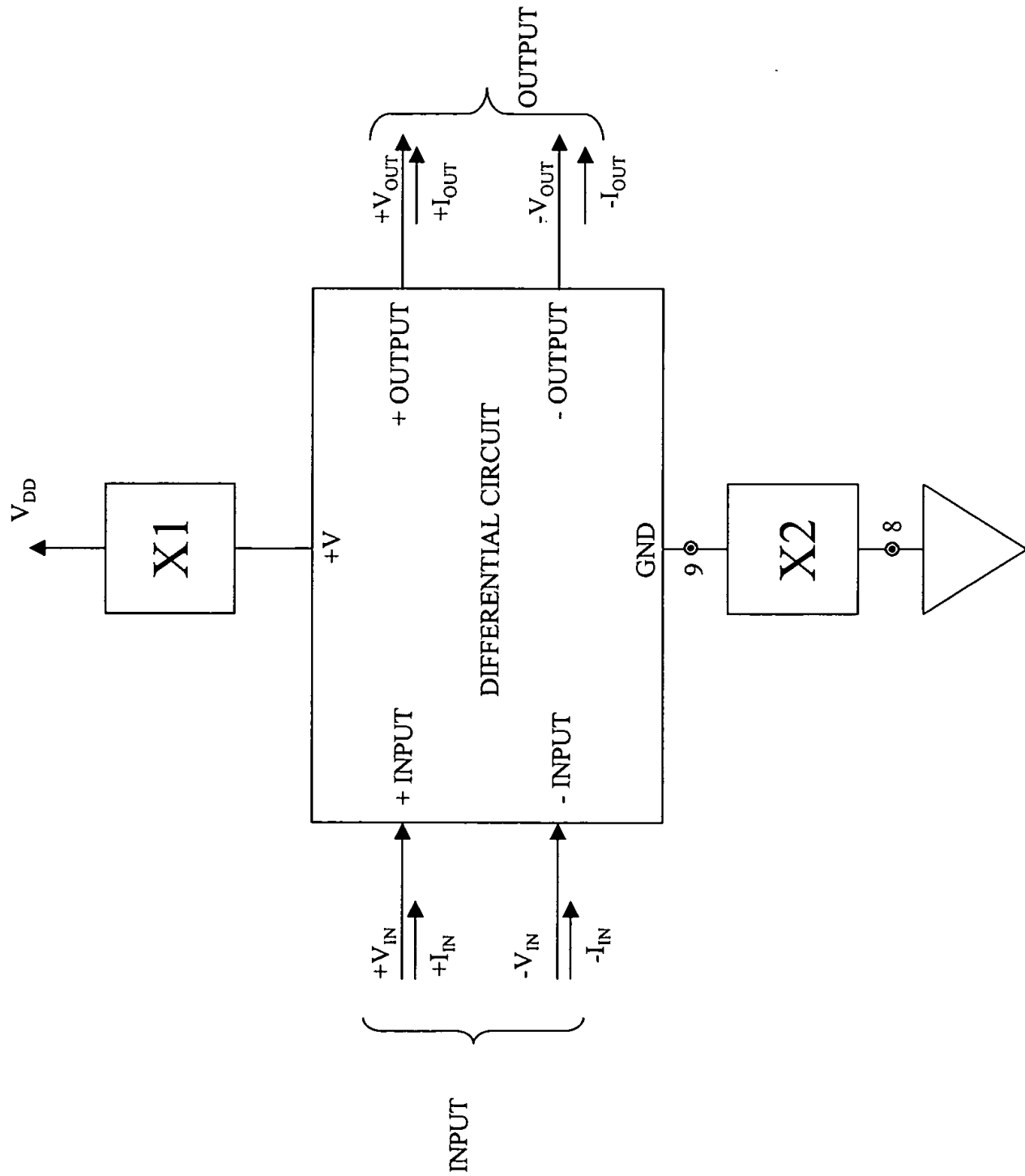


FIG. 48c

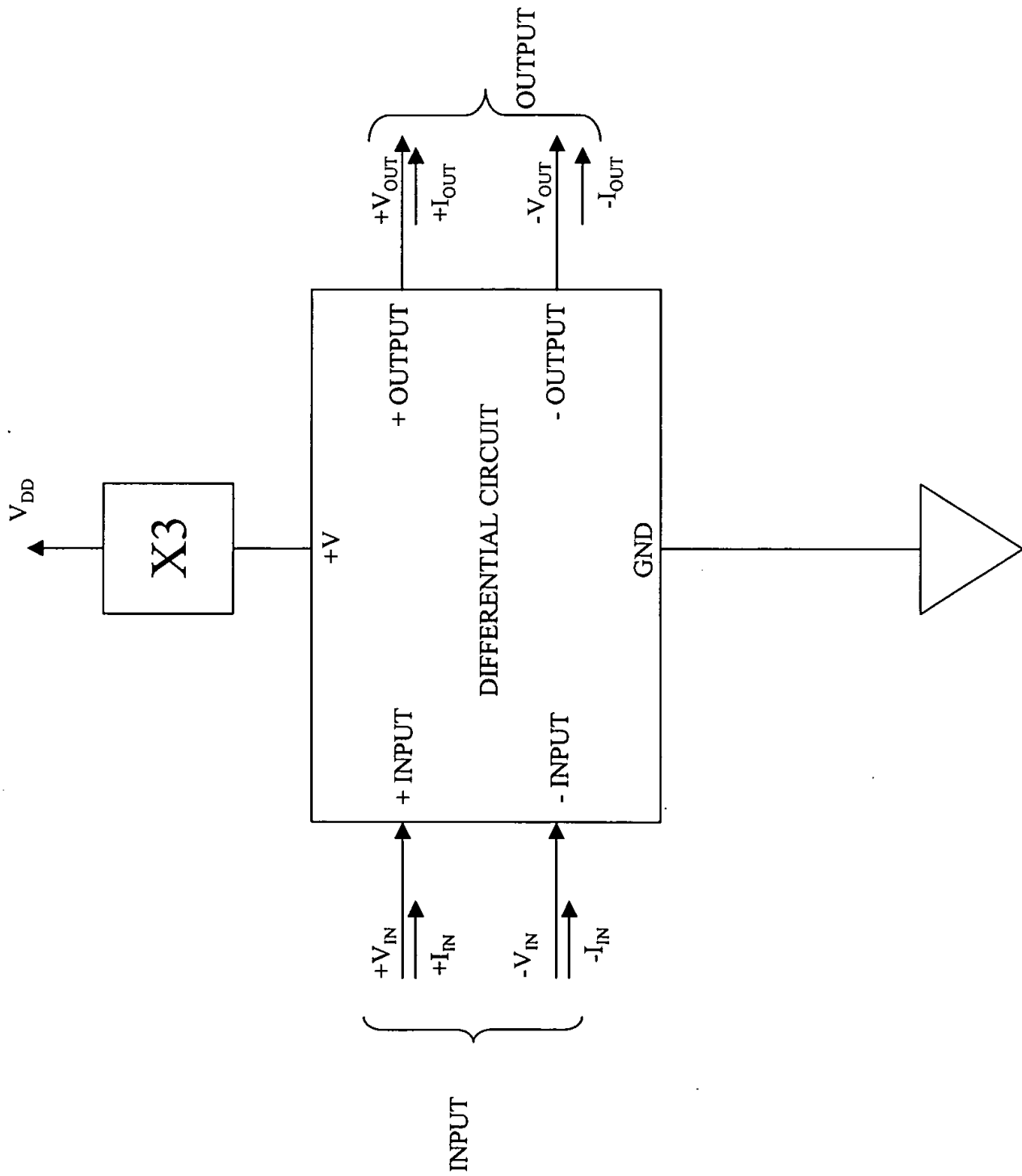


FIG. 48d

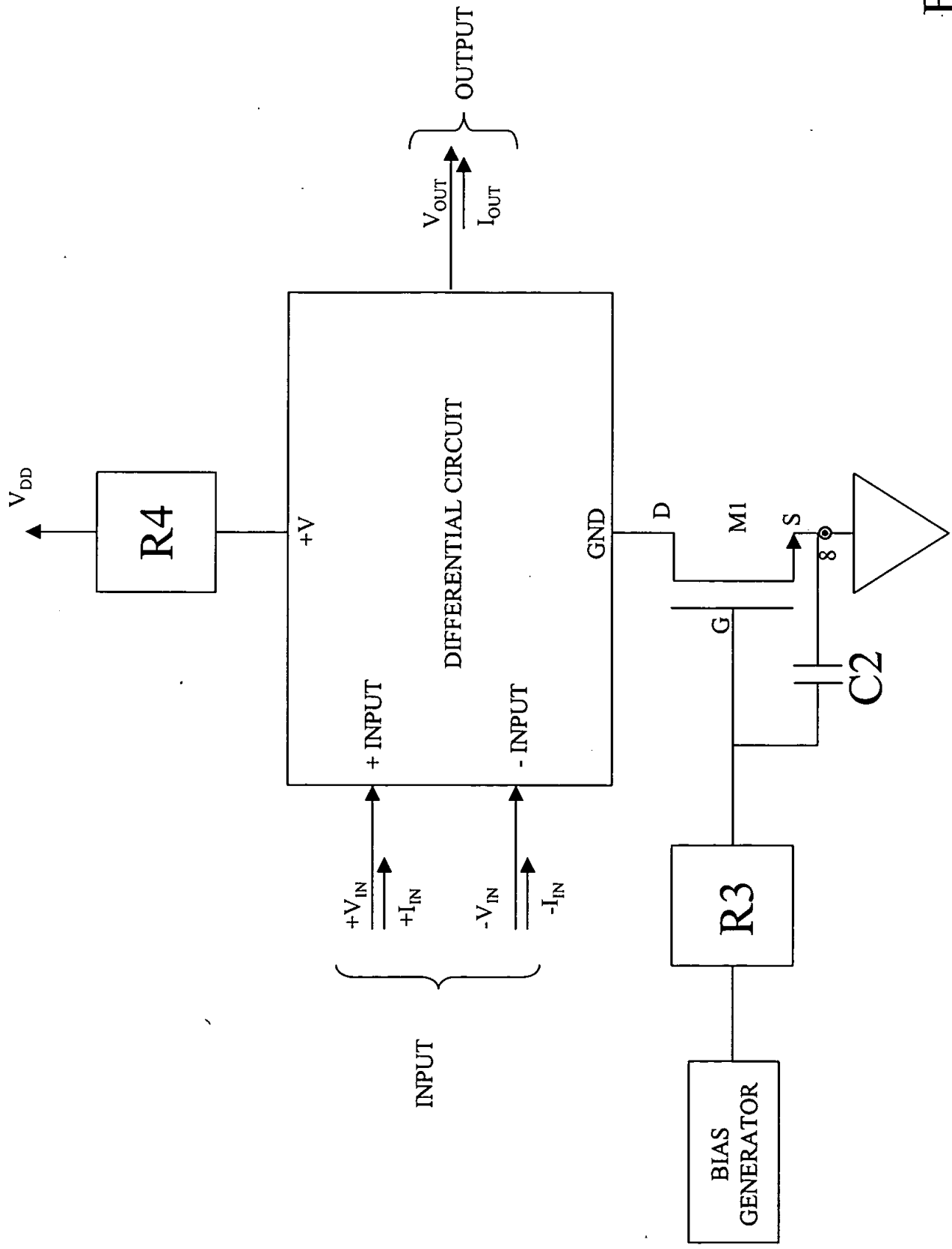


FIG. 40e

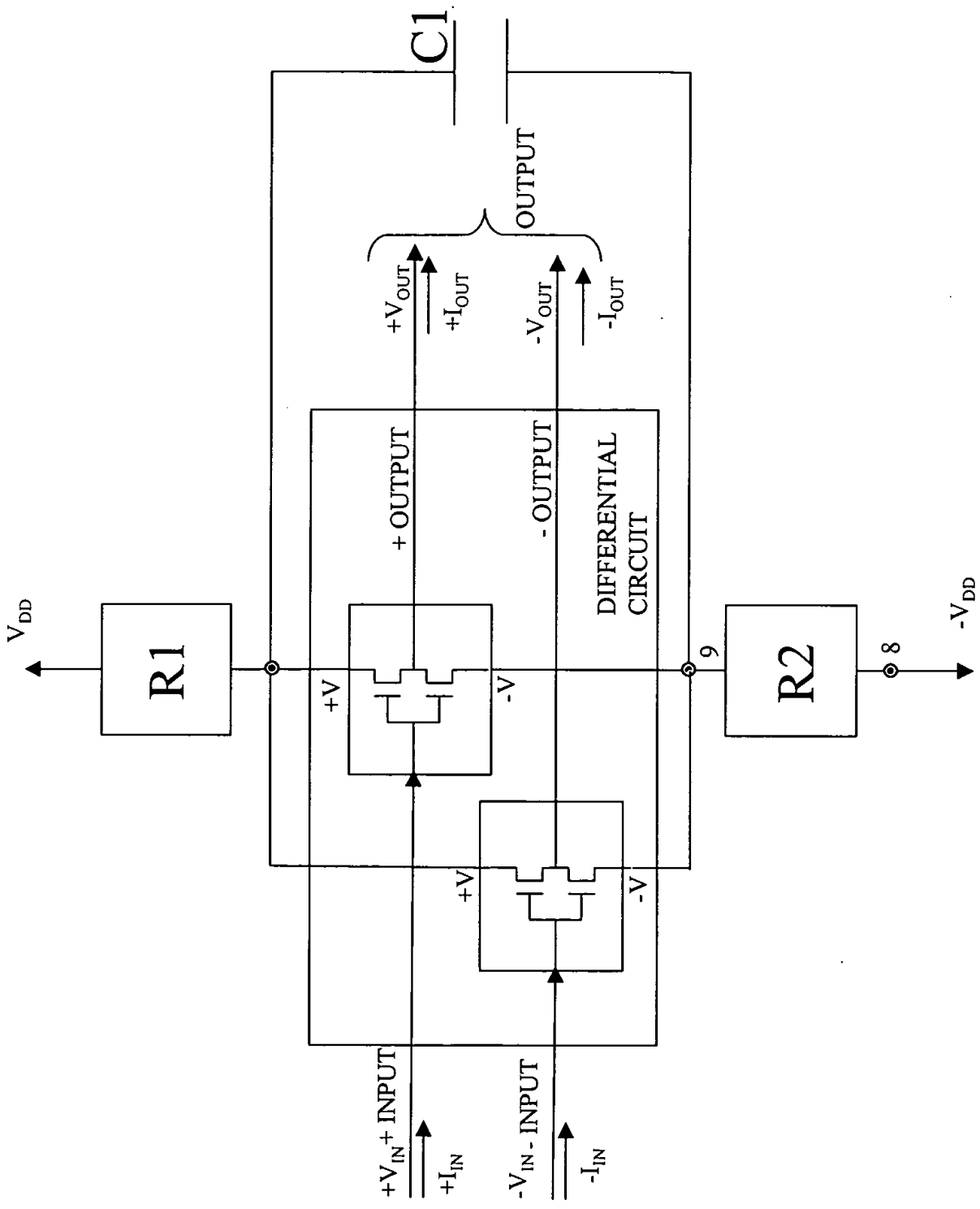


FIG. 48f

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